Advanced High Efficiency Architectures for Next Generation Wireless Communications

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Advanced High Efficiency Architectures for Next Generation Wireless Communications

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Turin, April 9, 2019

Summary

The world of wireless communications is in rapid evolution and communication service providers presently face several challenges related to the evolution to next generation (5G) networks. A major one is how to build the capacity required, while keeping the system as efficient and flexible as possible. Simultaneously, the increasing pervasiveness of the infrastructure calls for limited cost and complexity. In a microwave transceiver front end, the power amplifier present in the transmitting chain is often the bottleneck to the overall system efficiency and, at the same time, it strongly affects linearity.

This thesis is split into two focus areas, each facing some of these challenges from a different perspective of the design and operation of power amplifiers. The first part analyses some solutions that involve the circuit- and system-level architecture. Two power amplifier architectures based on load modulation, which aim at enhancing the efficiency of transmitters operating with envelope modulated signals, are investigated, realised and experimentally characterised. The design of a Chireix outphasing transmitter is first presented, based on the guidelines extracted from a simplified analysis on the bandwidth limiting factors. It is observed that the device parasitics often represent the main limitation to the achievable bandwidth, and some design strategies are proposed to partially overcome this issue. Secondly, the Doherty architecture is investigated from the point of view of its driving strategies. A comparison of analogous single and dual-input Doherty amplifiers is carried out with the aim of quantifying the trade-off between the advantages of the dual-input architecture in terms of performance and flexibility, and the increase of cost and complexity brought about by its employment in place of the conventional single-input one.

The two architectures based on load modulation are manufactured adopting packaged GaN transistors suitable for S-band (2–4 GHz) operation and power levels of few tens of watts. When higher frequencies are targeted for the same power levels, MMIC realisations are called for. GaN HEMT processes exist that enable the achievement of such performance, but at a significantly higher cost than GaAs pHEMTs, which however have lower breakdown voltages and therefore lesser power capabilities. Hence, the second part of this thesis is dedicated to developing cost effective architectures that may replace a single active device with high frequency

and high power capabilities. In this framework, the stacked architecture is analysed to exploit a GaAs multi-transistor structure whose performance is comparable to a single GaN device, at a lower cost. The strategy of stacking several transistors in such a way as to overcome the breakdown limit of a single one, which is already quite popular in CMOS, is gaining increasing interest for compound semiconductors, though with several challenges both from the stability and from the layout compactness points of view. The concept is verified by a MMIC cell meant for source and load pull characterisation.

Further investigation of each topic is planned as future development. Concerning the two dual-input load modulation architectures, system level characterisation is still ongoing, targeting a fully LUT based approach that enhances flexibility and potentially allows to embed linearisation into the signal conditioning itself. Eventually, the development of GaAs stacked transistor cells with high frequency performance comparable to GaN devices can be merged with the explored complex efficiency enhancement architectures to realise a cost-effective transmitter front end, suitable for next generation wireless systems.

Acknowledgements

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To my family and to Andrea, whose constant presence and support, sometimes apparent and very often silent, patient and affectionate, have been essential for the successful outcome of this PhD.

There is a bit of you all in this thesis, believe it or not.

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Acronyms

AM-PM Amplitude Modulation–Phase Modulation.

CMOS Complementary Metal Oxide Semiconductor.

CW Continuous Wave.

DC Direct Current.

DPA Doherty Power Amplifier.

DPD Digital Pre-Distortion.

EER Envelope Elimination and Restoration.

ET Envelope Tracking.

FET Field Effect Transistor.

FOM Figure Of Merit.

GaAs Gallium Arsenide.

GaN Gallium Nitride.

HEMT High Electron Mobility Transistor.

HEPR High Efficiency Power Region.

IIN Impedance Inverting Network.

IMN Input Matching Network.

InGaAs Indium Gallium Arsenide.

LMBA Load Modulated Balanced Amplifier.

LTE Long Term Evolution.

LUT Look-Up Table.

MIMO Multiple-Input Multiple-Output.

MMIC Monolythic Microwave Integrated Circuit.

OBO Output power Back-Off.

OFDM Orthogonal Frequency-Division Multiplexing.

OMN Output Matching Network.

PA Power Amplifier.

PAE Power Added Efficiency.

PAPR Peak-to-Average Power Ratio.

pHEMT Pseudomorphic High Electron Mobility Transistor.

PM-AM Phase Modulation–Amplitude Modulation.

RF Radio Frequency.

RFID Radio Frequency Identification.

Si Silicon.

SiC Silicon Carbide.

Chapter 1

Introduction

1.1 Background and motivation

1.1.1 Challenges in microwave PA design

One of the challenges of wireless communications nowadays is the achievement of increasingly high data rates for a given channel bandwidth, while keeping the transmission power level as limited as possible thus maximising efficiency. Table 1.1 summarises the requirements of the latest communication standards in terms of modulation scheme and corresponding data rate. In agreement with the trend noticeable from 3G to 4G, the latest generation (5G) is forecast to demand data rates several orders of magnitude higher than the current one. This poses a challenge in terms of infrastructures as well as system requirements [1, 2]. A large number of smaller-sized base stations are to be deployed, together with the adoption of advanced air interface solutions (e.g., Multiple-Input Multiple-Output (MIMO)) and the exploitation of new portions of the electromagnetic spectrum, including millimetre-wave frequencies. Besides these strategies, an already ongoing trend is the adoption of non-constant-envelope modulation schemes with increasingly high PAPR, hence the stringent need to improve back-off PA efficiency even further.

Significantly different power levels are handled by the components of a wireless mobile network. PAs for handsets must typically provide output powers below 1 W, while 100 W–200 W are required for a medium-sized 3G/4G base station. Microwave backhaul links below 40 GHz handle up to 10 W, and similar values are expected for future small-sized 5G base stations [3], while a few watts may be sufficient if higher frequencies are adopted [4]. However, achieving the required power levels along with a sufficiently high gain is quite demanding at frequencies above 15 GHz. Moreover, the adoption of multi-carrier modulation schemes and the continuous increase of baseband signal bandwidths are currently making it a great challenge to simultaneously obtain highly efficient and wideband PA operation [5].

The efficiency of a PA strongly depends on the technology of the active devices

on which it is based. Technological advances, such as the down-scaling of their physical dimensions and the development of processes based on innovative materials with highly engineered performance, have played a crucial role in increasing efficiency at high frequency.

This work is focused on medium/high-power applications at frequencies above 1 GHz, for which the two viable technological solutions are Gallium Arsenide (GaAs) Pseudomorphic High Electron Mobility Transistor (pHEMT) and Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) processes. Despite its higher cost with respect to GaAs, GaN technology is attracting major interest due to its higher breakdown voltage, which allows the devices to sustain high power levels with reduced area occupation [6, 7].

The maximum efficiency of a single stage power amplifier depends on the Direct Current (DC) power consumption, which in turn is related to the bias point of the device. This, together with its harmonic loading, determines the class of operation of the active device [8, 9]. Reduced conduction angle (e.g. class C), switching mode (e.g. class E) and harmonically tuned (e.g. class F) PAs can provide high efficiency, but limited to peak power and at the cost of reduced linearity. Most of the conventional high-frequency PAs adopt devices biased in class AB, which are turned off for less than half of a period of the input signal. This usually provides a satisfactory trade-off between efficiency, gain and linearity [10]. However, it should be noted that even highly efficient PA classes only enhance the peak efficiency, which is achieved at maximum output power, whereas they have limited impact on back-off efficiency. Furthermore, they are typically based on resonant elements and tuned filters, thus resulting in narrowband behaviour.

1.1.2 Back-off efficiency issue

Current communication standards can provide high data rates in a limited frequency band thanks to the adoption of spectrally efficient modulation schemes. Signals adopting such modulations are characterized by a very high PAPR, meaning that the occurrence of peaks significantly higher than the average value in the time domain waveform is limited, as shown in Fig. 1.1. The PA efficiency is determined by the average output power. However, high linearity is also often required to the PA in order not to distort the output signal up to the point where the quality of the carried information is compromised. For instance, the PA must not clip the signal peaks, meaning that the maximum output power of the PA must be approximately PAPR times larger than the average one. Crest reduction techniques [11, 12, 13] can be applied to partially overcome this limit.

Table 1.1: Features of wireless communication standards.

Gener.	**Standard**	**Interface and Modulation**	**Max. Freq.**	**BW**	**Max. PAPR**
			GHz	MHz	dB
2G	GSM/EDGE	TDMA/FDMA, GMSK, 8PSK	1.9	0.2	3.3
3G	UMTS	W-CDMA, QPSK/64QAM	3	5	10.6
4G	LTE	OFDMA, MIMO-4x4, 64QAM	5.9	20	12
	LTE-Advanced	OFDMA/SC-FDMA, MIMO-8x8, CA, 64QAM	5.9	20/100* (* with CA)	12
	WiMAX	OFDMA, MIMO-2x2, QPSK/64QAM	5.8	20	12
5G	5G	OFDMA, HetNet, massive MIMO, advanced CA, CoMP, ...	40	>100 (800–2000)	>12
3G/4G backhaul	point-to-point	4096QAM	86	56	12

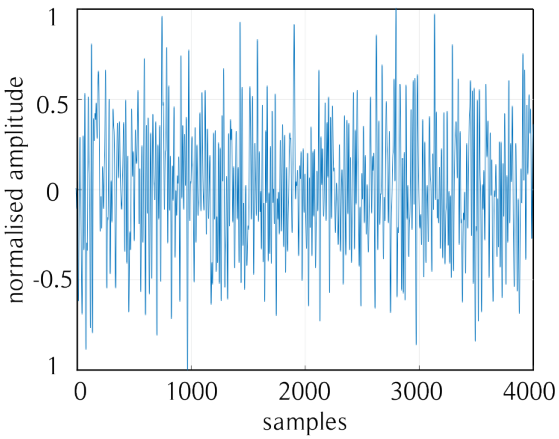


Figure 1.1: Waveform of a 5MHz OFDM LTE signal with 10 dB PAPR.

Fig. 1.2 reports the efficiency of a conventional class AB PA along with the probability density functions of three different modulated signal, as a function of OBO, which is the amount of output power reduction with respect to the maximum expressed in dB. Class AB efficiency is monotonically increasing as a function of the output power. Therefore, the amplifier exhibits high average efficiency only if the average power of the signal to be amplified is reasonably close to the maximum one. This is the case for low-PAPR signals, e.g. those adopting GSM modulation, shown

in grey in Fig. 1.2. However, in the case of high-PAPR signals (e.g. LTE, shown in red), the PA is operated at high OBO levels during most of the transmission, leading to an average efficiency that is only a small fraction of the maximum one.

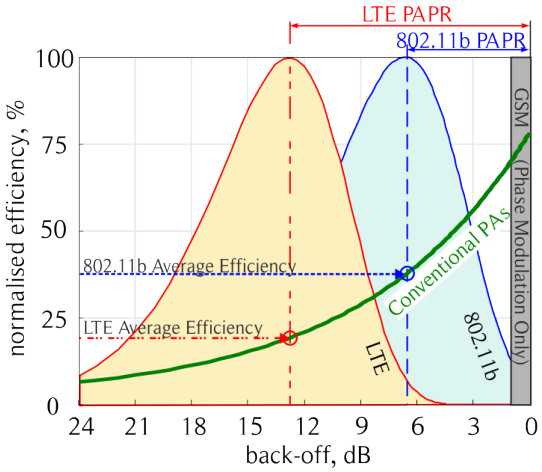


Figure 1.2: Efficiency of a class AB PA (green) compared to the probability density function of different types of modulated signals: GSM (grey), 802.11b (blue) and LTE (red).

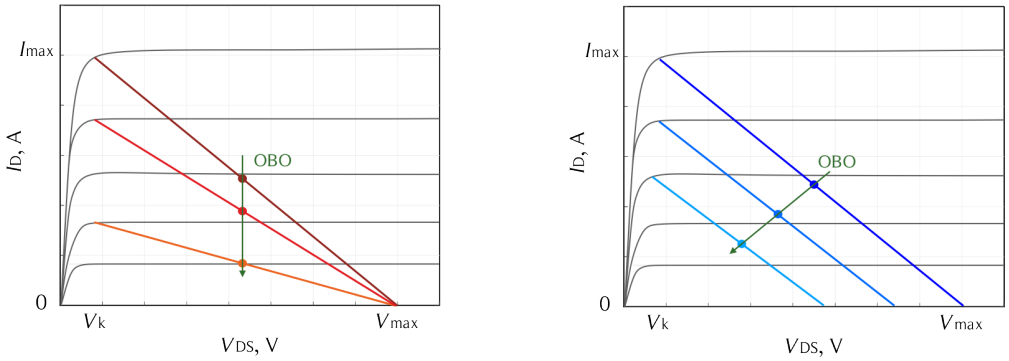
1.2 Back-off efficiency enhancement

For a given bias point, an active device is maximally efficient when both its output voltage and current swings are maximised. These swings are related to the load termination R_{L} and the drain supply voltage $V_{DS,0}$ as

$$V_{\mathrm{d}} = V_{\mathrm{DS},0} - I_{\mathrm{d}} R_{\mathrm{L}}.$$

The evolution of the output voltage and current in time can be visualized as a dynamic load line, as shown in Fig. 1.3. For a given power level, i.e. for a given I_{d}, it is possible to determine the optimum load which maximises the output swings, whose value is related to the slope of the dynamic load line. To ensure high efficiency at any possible back-off level, the load line should be dynamically changed as a function of the input power. As shown in Fig. 1.3, this can be done either acting on the load resistance or on the drain supply voltage, leading to two possible back-off efficiency enhancement approaches: load modulation and supply voltage modulation [8].

Some popular load modulation solutions are the Doherty [14] and the Chireix outphasing [15]. Concerning supply voltage modulation, the Envelope Elimination and Restoration (EER) technique, also known as the Kahn technique [16], and



(a) load modulation (b) supply modulation

Figure 1.3: Load lines for the load modulation (a) and supply voltage modulation (b) principles.

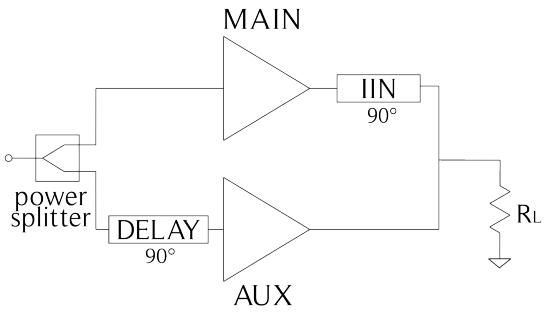
the Envelope Tracking (ET) [17] technique are currently attracting major interest. More recently, combinations of several of such techniques, such as asymmetric multilevel outphasing [18], have been also investigated.

Other efficiency enhancement techniques exist that fall outside this classification, for instance the Sequential Power Amplifier (SPA) [19, 20, 21], which however is outside the scope of this work.

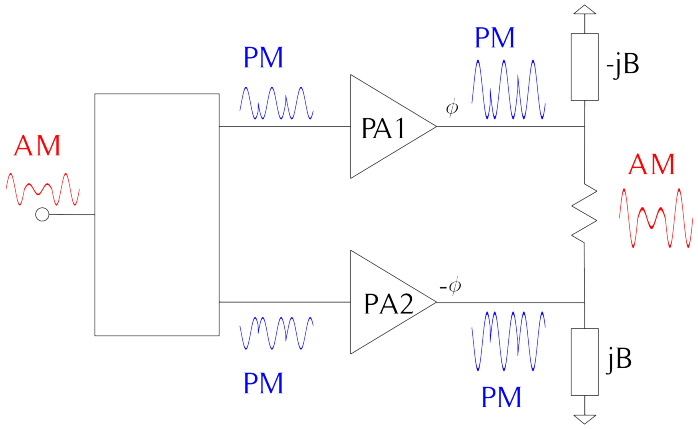
1.2.1 Load modulation

Load modulation is a popular strategy to enhance the PA efficiency in back-off. The Radio Frequency (RF) signal injected by a source sums to the RF output of the PA itself and modifies its load impedance dynamically, thus making it possible to extend high efficiency operation region. Several efficiency enhancement techniques were invented in the early 1900s, at the beginning of the era of radio broadcasting. The main motivations behind this research effort were thermal issues and running costs of transmitters handling tens of kilowatts.

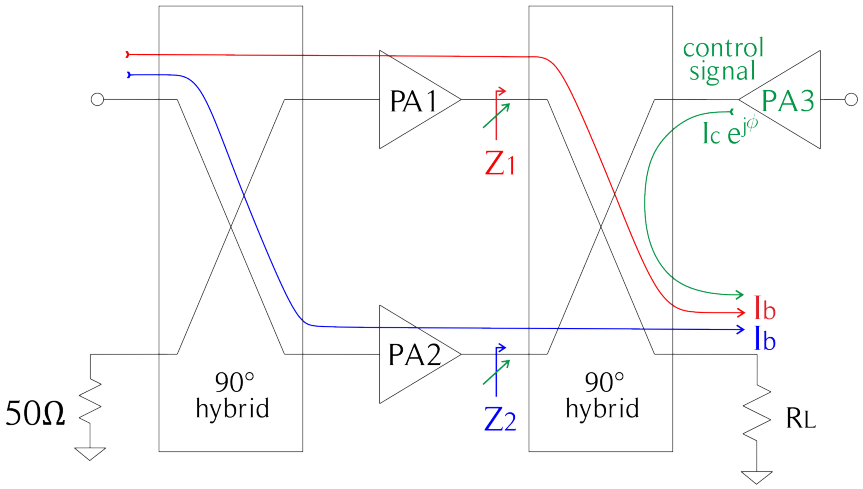
The Doherty and Chireix outphasing, as well as the more recent Load Modulated Balanced Amplifier (LMBA), belong to this category. The Doherty and Chireix outphasing architectures both date back to the early '90s [14, 15]. They are originally two-PA architectures, although their working principle can be extended to more than two PAs. In the Doherty architecture, the two PAs are not on the same hierarchical level. An *auxiliary* PA injects a current of appropriate amplitude and phase at the common node between the *main* PA and the load. If properly designed, the main load can be modulated from the optimum value at saturation to a larger value in back-off. On the contrary, the two PAs can be considered "peers" in the Chireix outphasing architecture. They are both connected to a common load, and they are assumed to work as ideal voltage sources of equal



(a) Doherty



(b) Chireix outphasing



(c) LMBA

Figure 1.4: Block diagrams of the load modulation architectures.

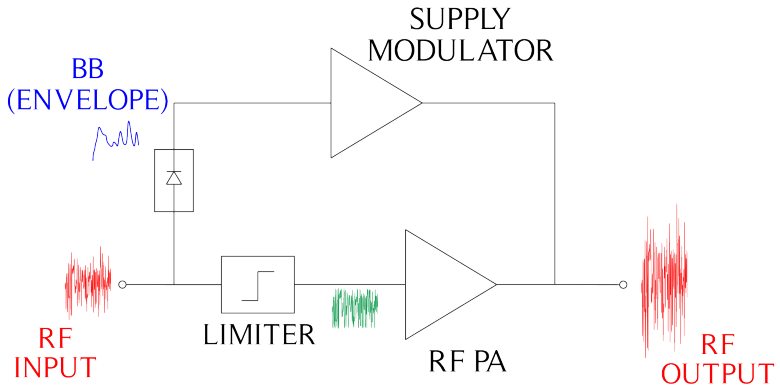
and constant amplitude, and opposite phase.
A more recent architecture that exploits the load modulation principle is the LMBA

[22]. It is a sort of evolution of the conventional balanced amplifier where the output port, which is usually terminated on 50 Ω is instead used to inject an RF signal generated by another source. It is natively a three-PA configuration in which a third *ancillary* RF signal source modulates the load of the two identical PAs in the balanced configuration. Under this perspective, the LMBA working principle is more similar to that of the Doherty rather than the Chireix, because one of the PAs acts as an active load to the other(s).
The working principle of Doherty and Chireix outphasing architectures is dealt with in the following chapters, whereas the LMBA is just mentioned here for the sake of completeness but is not an object of this dissertation.

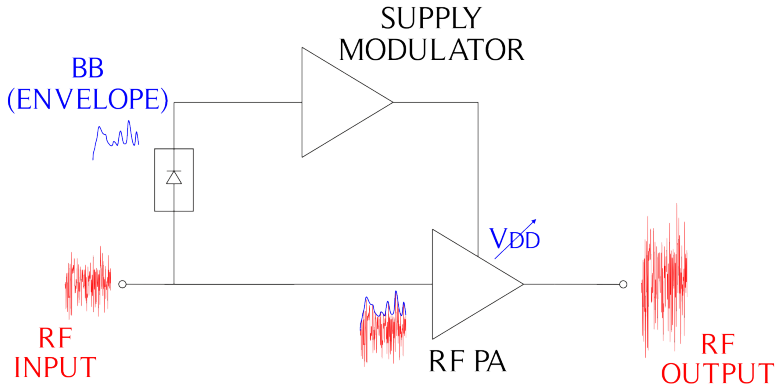
1.2.2 Supply voltage modulation

Dynamically adapting the supply voltage of a PA according to the average value of its RF input signal is a popular strategy to maintain high efficiency over a wide dynamic range. It may be seen as a system level solution that is, at least in principle, applicable to any PA or multi-PA architecture by adding the envelope detection and amplification elements required to dynamically adjust the supply voltage. One of the techniques that rely on this principle, referred to as EER, was first invented by L. R. Kahn in 1952 [16] and has recently been rediscovered and developed, especially for telecommunication applications [17]. The EER technique is based on the combination of a non-linear but highly efficient RF PA and an envelope supply modulator, which are sketched in Fig. 1.5 (a). The input signal, containing in general both amplitude and the phase information, is split into an envelope path and an RF path containing the constant-envelope phase-modulated signal. While the highly efficient RF PA amplifies the constant-envelope signal, the supply modulator provides an high-power signal proportional to the envelope of the input signal. This modulates the power supply of the RF PA, thus restoring the signal envelope and producing an amplified replica of the input signal. The EER transmitter is ideally both linear and highly efficient. Because the RF PA is always saturated, it operates at the maximum efficiency, thus making the average system efficiency significantly higher than that of conventional transmitters. Analogously to the case of outphasing transmitters, the linearity of EER transmitters does not depend on the linearity of the RF PA, but rather on that of the supply modulator. In fact, the challenging bandwidth and efficiency requirements of the supply modulator make EER less attractive for broadband applications [17].

ET is an alternative technique based on the same principle. It employs a linear RF PA which does not have extremely high efficiency in itself, but which is driven in its high-efficiency region by adjusting the supply voltage accordingly thanks to the adoption of a supply modulator. There is a substantial difference between ET and EER, which is highlighted in Fig. 1.5 (b). In the former, no limiter is employed and consequently the RF PA amplifies an envelope modulated signal, whereas in



(a) EER



(b) ET

Figure 1.5: Block diagrams of the supply voltage modulation architectures.

the latter the RF signal has constant envelope.

This introductory overview of the back-off efficiency challenge in PAs for modern wireless communications has led to the publication of [23], which is a review of the most popular efficiency enhancement techniques based on load modulation.

1.3 Structure and objectives

This work addresses some major challenges in the microwave power amplification field by focusing on two levels, namely the system and device level.

Chapters 2 and 3 focus on the circuit/system level. The back-off efficiency enhancement issue is addressed by focusing on two aspects, both related to the

bandwidth achievable by a specific PA architecture. As far as the Chireix outphasing architecture is concerned, an investigation of the bandwidth limiting factors is carried out with the aim of deriving simple guidelines for the design. Concerning the Doherty architecture, rather than focusing on the design of the amplifier itself, the focus is moved to the driving strategies and the possible performance enhancement brought about by the dual-input solution as opposed to the conventional single-input. In both cases, the manufactured experimental prototypes are hybrid ICs based on packaged GaN HEMTs and target S-band operation (2–4 GHz) with power levels of few tens of watts.

Finally, one of the technological challenges faced by modern telecommunications systems is addressed in Chapter 4, which focuses on the device level. The stacked topology is presented and applied to GaAs HEMTs in MMIC implementation, in an attempt to find a cost effective alternative to GaN for high-frequency (above 10 GHz), medium-to-high power applications.

Chapter 2

The Chireix Outphasing Architecture

The term Chireix outphasing does not indicate a PA in itself, but rather a two-way (or, more in general, N-way) architecture that combines PAs in parallel by means of a non-isolating combiner. The system achieves high efficiency operation over a wide output power range thanks to an appropriate compensation of the unwanted dynamic reactive part of the complex load presented to each branch. As the back-off efficiency peak is related to the proper design of the shunt compensation elements, which resonate out the load reactances, it could be argued that the Chireix outphasing architecture is intrinsically narrowband. It must be noted, however, that the compensation elements are not the only factors that affect the bandwidth achievable by the system. In fact, the non-isolating output combiner, as well as the device parasitics, also contribute to limiting the bandwidth. Wideband designs exist in the literature, but they are based on approaches that are not limited to the "pure" outphasing. In [24], for example, a continuum between the Doherty and outphasing modes of operation is identified and exploited to design a PA achieving 6 dB back-off PAE larger than 45 % from 1 to 3 GHz, thus reaching the 100% fractional bandwidth target. On the other side, in [25] outphasing is used together with discrete level supply modulation.

On the contrary, this chapter focuses on "pure" Chireix outphasing PAs. The work, which was presented at the 13$^{\text{th}}$ European Microwave Integrated Circuits Conference (EuMIC) in Madrid in 2018 [26], is based on a systematic assessment of the bandwidth limiting factors in a simplified model of the output section of an outphasing system. The bandwidth analysis is explained in detail in 2.2. The design of the prototype, presented in 2.3, is led by topological choices made based on this assessment. In particular, the design of the output combiner is led by the observation that the output parasitic elements of the selected active device pose the most severe limitation to the overall bandwidth.

2.1 Theory and practical implementations

2.1.1 Terminology

Before entering into details of its operation, a few remarks on the terminology are called for. The term outphasing is currently found in the literature to refer to different architectures, which all exploit the power combination of two signals with equal amplitude and opposite phase but differ in the way the combination itself is implemented. Ultimately, this has a significant effect on the performance of the overall system. The combination of two RF sources with a variable differential phase to generate an amplitude modulated signal is not the novelty of the Chireix architecture. In fact, it was widely used in AC systems [27]. The term *outphasing* can in general refer to a PA architecture that combines two signals by means of a standard (isolating) Wilkinson-like power combiner, which delivers the in-phase component to the load and dissipates the quadrature component on the resistor. As such, the load seen by each of the input ports is fixed as the phase difference between the two input signals varies. It immediately follows that the phase-efficiency curve of such a system drops steeply as the phase unbalance (the outphasing angle ϕ) increases, reaching zero when ϕ equals 180°. In fact, the major advantage of such architecture is not at all its efficiency, but rather its linearity. As each branch PA works at a fixed power level, no distortion should in principle affect the signal. In 1935, Chireix claimed a substantial modification to the generic outphasing architecture introduced above: the introduction of a non-isolating power combiner [15]. The two branches are no longer isolated. On the contrary, each modulates the load seen by the other. Chireix realised that it is possible to cancel the reactive part of the load impedances at a specific working condition (i.e. for a specific value of the outphasing angle ϕ) by introducing appropriate shunt compensating elements. Therefore, the peculiarity of the Chireix architecture is to have an efficiency peak at a specific back-off point, i.e. to reduce the DC power consumption of the PAs at a given out-of-phase condition, when the vectorial sum of their output signals is nearly null and the system is generating a signal at the low end of the dynamic range. Such architecture will be referred to as "Chireix outphasing". Recent works found in the literature are alternatively identified as "Chireix", "Chireix outphasing" or simply "outphasing". Despite the different denomination, which is often due to the absence of a generally recognised convention, these architectures typically make use of a non-isolating power combiner and a load compensation network, which can have several possible implementations.

2.1.2 Theoretical foundations

As reported in [8], the basic working principle of any outphasing system can be effectively summarised and synthetically illustrated by any of the trigonometric

formulas known as sum-to-product, such as:

$$\cos(A) + \cos(B) = 2\cos\left(\frac{A+B}{2}\right) \cdot \cos\left(\frac{A-B}{2}\right). \tag{2.1}$$

To make its meaning clearer in this particular framework, one should take the generic terms to be time domain signals of the form $\cos(A(t)) = \cos(\omega t + \phi(t))$ and $\cos(B(t)) = \cos(\omega t - \phi(t))$ If read left-to-right, (2.1) says that the sum of two oppositely phase modulated signals having the same amplitude is an amplitude modulated signal:

$$\cos(\omega t + \phi(t)) + \cos(\omega t - \phi(t)) = 2\cos(\phi(t)) \cdot \cos(\omega t) = 2a(t) \cdot \cos(\omega t). \tag{2.2}$$

It should be noted that the Phase Modulation–Amplitude Modulation (PM-AM) relation is not linear; in fact, $a(t) = \cos(\phi(t))$. Moreover, the resulting signal has no phase modulation unless a common mode phase modulation $\varphi(t)$ existed in the input signals, in which case this would be transferred to the output unaffected:

$$\cos(\omega t + \phi(t) + \varphi(t)) + \cos(\omega t - \phi(t) + \varphi(t)) = 2\cos(\phi(t)) \cdot \cos(\omega t + \varphi(t)). \tag{2.3}$$

Up to now, the fairly simple mathematics illustrates a system in which a combiner performs the vectorial sum of two branch signals with differential phase modulation and reconstructs an amplitude modulated output signal on the load. This is the origin of the outphasing architecture for PAs. Furthermore, reading (2.1) right-to-left suggests the possibility of realising the dual-input structure: a splitter that takes an amplitude modulated signal as input and generated two signals whose amplitude is equal and constant and whose phase modulation is opposite. This would theoretically allow one to build a complete single-input single-output system with a given AM-AM transfer characteristic, which could thus be characterised as a *macro-PA*. Despite some successful attempt in recent years [28, 29], the realization of an analog input phase modulator following the inverse law as the Chireix combiner is extremely challenging. The Chireix outphasing system which will be analysed throughout this chapter is a dual-input system preceded by a digital signal processing stage in charge of generating the appropriate branch driving signals.

2.1.3 Non-isolating combiners

In the original Chireix's paper, the outphasing devices are loaded with a common, differentially connected resistor. This implicitly acts as a non-isolating combiner, which sums the output voltage vectors. The analysis of the equivalent circuit of the output section of an outphasing system shown in Fig. 2.1 assumes the two branch PAs to behave as ideal voltage sources whose amplitude is equal and constant and whose phase is modulated in an opposite way, i.e. $V_1 = Ve^{\phi}$ and

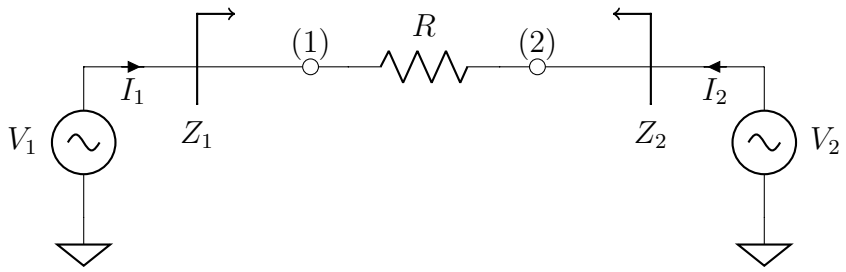


Figure 2.1: Differential load.

$V_2 = Ve^{-\phi}$. Defining the impedance seen by branch i as $Z_i = V_i/I_i$, and $Y_i = 1/Z_i$ the corresponding admittance, leads to the series equivalent representation

$$Z_{1,2} = \frac{R}{2} \cdot [1 \mp \mathrm{j}\cot(\phi)] \tag{2.4}$$

or, alternatively, to the parallel representation

$$Y_{1,2} = \frac{1}{R} \cdot \left[2\sin^2(\phi) \pm \mathrm{j}\sin(2\phi)\right]. \tag{2.5}$$

The differential load representation of Fig. 2.1 is often employed in recent works when the analysis of a simplified structure is necessary. However, planar technology used to realize solid-state amplifiers does not allow for a direct implementation of such topology. The output of each branch amplifier is typically a single-ended signal, which can be connected to a differential load by means of a balun or a transformer [30]. Alternatively, a *Wilkinson type* combiner based on $\lambda/4$ TL sections (Fig. 2.2) may be conveniently implemented both with lumped coaxial cables and in planar technology, e.g. microstrip. This transforms voltage sources into current sources, whose currents are summed in the common node where the single-ended load is connected [30]. Note that, unlike the true Wilkinson structure shown in Fig. 2.3, which acts as an isolating combiner in that it sums the in-phase signal contributions while dissipating on the resistor the quadrature components, the *Wilkinson type* non-isolating combiner has no resistor across the symmetric ports. The dynamic load impedance presented to each branch with isolating and non-isolating Wilkinson combiner are derived in the following. The equivalent $\mathbf{Y}$ matrix of the 2-port in Fig. 2.2, which can be derived using standard TL theory, is

$$\mathbf{Y} = \frac{R}{Z_\infty^2} \begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix}. \tag{2.6}$$

By solving the corresponding system with the proper values for V_1 and V_2

$$I_1 = I_2 = \frac{R}{Z_\infty^2} V(e^{\phi} + e^{-\phi}) \tag{2.7}$$

one derives

$$Y_{1,2} = \frac{R}{Z_\infty^2}\left[2\cos^2(\phi) \mp \mathrm{j}\sin(2\phi)\right]. \tag{2.8}$$

If the isolating resistance $R_\mathrm{w} = 2R$ is added, and $Z_\infty = \sqrt{2}R$, the topology behaves as a conventional Wilkinson whose ports are all matched to R. In this case, the resulting matrix $\widetilde{\mathbf{Y}}$ of the 2-port can be derived from $\mathbf{Y}$ by inspection:

$$\widetilde{\mathbf{Y}} = \begin{bmatrix} Y_{11} + \frac{1}{R_\mathrm{w}} & Y_{12} - \frac{1}{R_\mathrm{w}} \\ Y_{21} - \frac{1}{R_\mathrm{w}} & Y_{22} + \frac{1}{R_\mathrm{w}} \end{bmatrix} = \frac{1}{R}\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}. \tag{2.9}$$

This immediately shows that $Z_1 = Z_2 = R$ independently of ϕ, i.e no load modulation occurs. In both of the topologies in Fig. 2.1 and Fig. 2.2, by connecting to

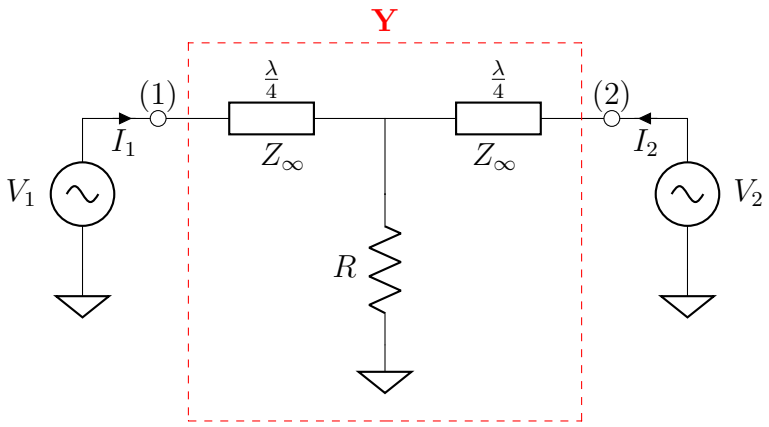


Figure 2.2: Non-isolating Wilkinson type combiner.

the combiner inputs two equal and opposite shunt reactances $\mp\mathrm{j}B$, a second efficiency peak arises at a given back-off level corresponding to an angle ϕ_c such that $B = \mathrm{Im}\{Y_1(\phi_\mathrm{c})\} = -\mathrm{Im}\{Y_2(\phi_\mathrm{c})\}$, while the original peak moves slightly away from the maximum power condition. In fact, (2.5) and (2.8) show that, if $Y_{1,2}$ are purely real for a given ϕ_c, then they are such also for $90° - \phi_\mathrm{c}$. On the other side, they are no longer real for $\phi = 0°$ after the compensation elements are introduced. The behaviour of the differential load topology is illustrated in Fig. 2.4, for the uncompensated case (red curves) and for three different values of compensation reactances. Their value is either computed from (2.5) or derived from Fig. 2.4 (d), which reports the imaginary part of the admittance presented to branch 1 (solid) and 2 (dashed) as a function of the outphasing angle ϕ. The admittance representation is particularly suited for the parallel compensation strategy adopted. The value of the compensation elements is $\mp\mathrm{j}\,B(\phi_\mathrm{c}) = \mp\mathrm{j}\,\mathrm{Im}\{Y_1(\phi_\mathrm{c})\}$, where $B = 34\,\mathrm{mS}$, $64\,\mathrm{mS}$, $87\,\mathrm{mS}$ for $\phi_\mathrm{c} = 10°, 20°, 30°$, which correspond to a power ratio $P_{\mathrm{R_L}}(\phi_\mathrm{c})/P_{\mathrm{R_L}}(90°)$ of 3%, 12% and 25%, respectively.

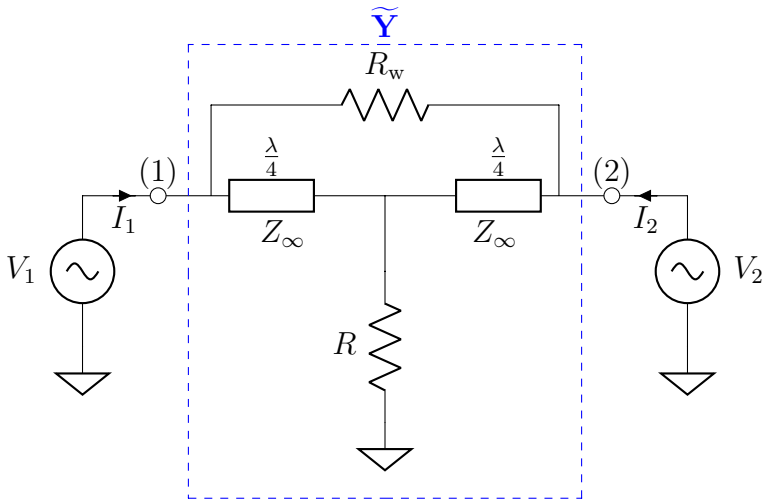


Figure 2.3: Isolating Wilkinson combiner.

While the load compensation network is made up by two equal and opposite shunt reactances connected to the combiner inputs in its original formulation, in 2007 Gerhard *et al.* proposed for the first time a solution to embed the load compensation into series TL sections, thus eliminating any shunt element [31]. The Wilkinson type combiner lends itself to such a modification, which merges the functions of power combination and reactive load compensation into the same physical element, leading to a TL-based combiner with sections of different lengths [32]. In particular, starting from the symmetric $\lambda/4$ structure, the equal and opposite compensating reactances are transformed into an equal and opposite variation $\pm\Delta$ of the TL length of the two branches. This configuration offers perhaps a limited possibility of tuning the circuit after realisation compared to the original one. However, in 2011, it was extended by Perreault to 4-way outphasing power combining, leading to an enhanced efficiency over a wide output dynamic range [33]. This positive effect is due to the fact that this new combiner provides nearly resistive loading of the individual power amplifiers over a very wide output power range, thus overcoming the loss and reactive loading problems of previous outphasing approaches. In fact, it has been shown that in traditional 2-way combining the reactive parts of the loads are only cancelled at two outphasing angles, and become large outside a relatively small neighbourhood of such points. This contributes to limiting the efficiency as a consequence of two factors: losses associated with added reactive currents, and performance degradation of the branch amplifiers under strongly reactive loading [30, 34]. Finally, a solution worth mentioning although not easily generalisable is that presented in [35]. Here the combiner has an arbitrary topology, selected empirically to synthesise the best fit to the 2-port parameters determined from load pull data. The prototype realised with 15-W bare die GaN HEMTs based

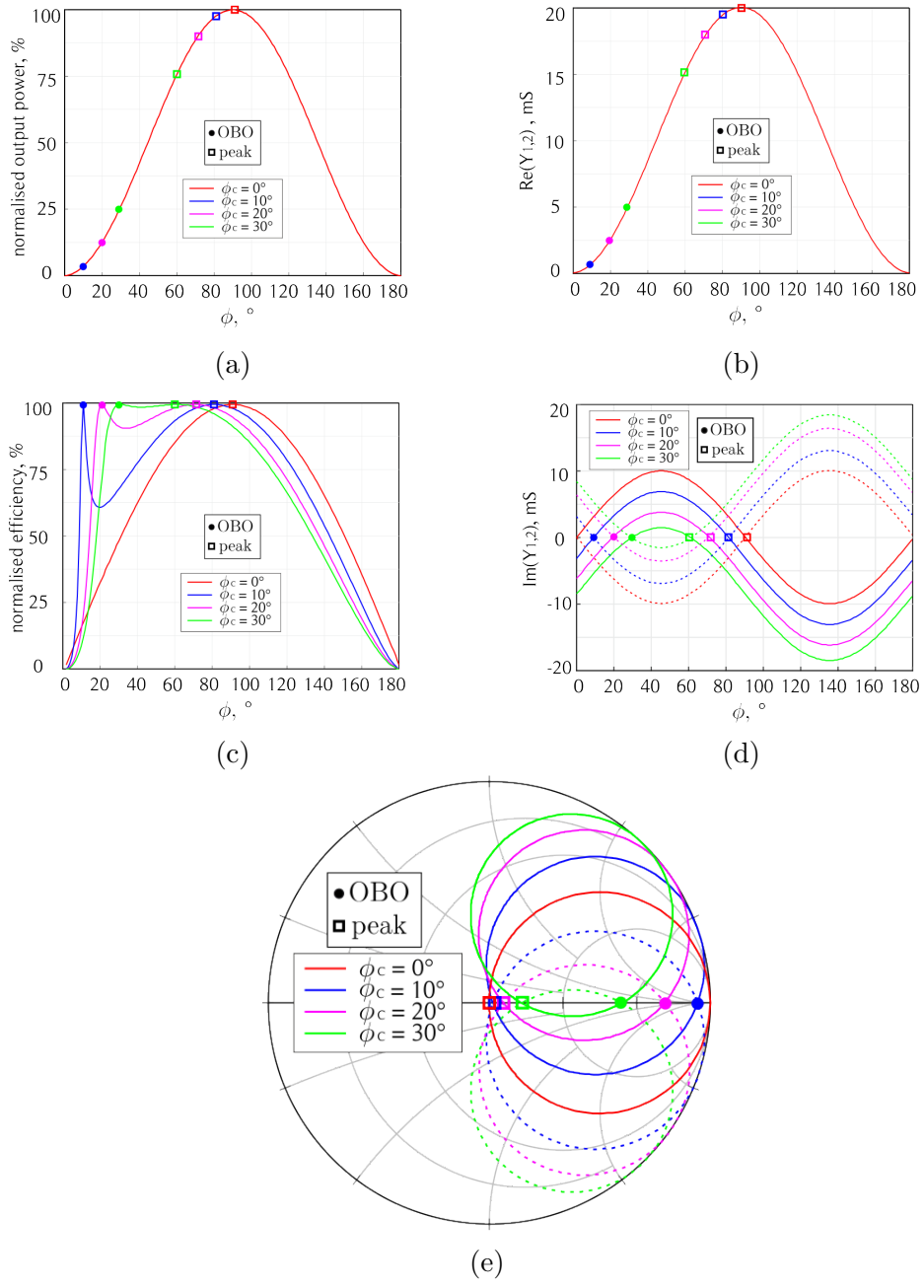


Figure 2.4: Simulated output power (a), efficiency (c), branch load impedances (b), (d) and corresponding reflection coefficients (e) of the differential load configuration in Fig. 2.1.

on this approach achieves a PAE in excess of 40 % and 20 % at peak power and 6 dB OBO, respectively, from 1.6 to 2.4 GHz.

Before reviewing the performance achieved by recently proposed works, it is

important to emphasize that the efficiency of an outphasing system as a whole depends on two factors, namely the PA efficiency and the combiner efficiency. As mentioned in [36], these can be treated as independent only up to some extent due to the interaction between the PA and combiner. In fact, when a non-isolating combiner is placed at the output of two outphasing PAs, the back-off PA efficiency is not improved compared to the analogous topology with an isolating combiner unless the reactive load compensation is also inserted. The combiner efficiency, on the contrary, is fixed to 100% in both cases, because no power is dissipated in the reactive part of load impedance. The amount of power that is not transferred to the load is reflected back to the PAs, which can either dissipate it or somehow store it by lowering the DC power consumption of the device, depending on the amplifier type. This is one of the factors concerning the reliability issue of outphasing systems due to the ability of the devices to withstand the stress caused by the very low loading in high outphasing conditions [27]. This reflected power could also be conducted away and rectified to generate DC power, analogously as in Radio Frequency Identification (RFID) applications [8, 37, 38, 39]. The addition of reactive compensation elements to the non-isolating combiner creates a second peak for the PA efficiency, which can be placed at the back-off level of interest.

2.1.4 Practical implementations

After its invention in 1935, the outphasing transmitter has somewhat recently been rediscovered. The potential advantages of such architecture are unravelled and analysed more in detail [30, 40, 41] and adapted to modern implementations, both for Megawatt-power low-frequency [42] and microwave [43, 44], applications. As far as the microwave field is concerned, several dual-input Chireix outphasing PAs have been presented in the past decades. The authors in [36] exploit saturated class B push-pull amplifiers based on GaAs HEMTs, achieving 3 W peak output power, combined though a Wilkinson combiner. The realised 2.14 GHz Chireix outphasing system achieves 42 % system efficiency with a 7 dB PAPR modulated signal. In [45], varactor tuning is applied to the popular topology based on a Wilkinson combiner complemented with shunt compensation elements. This enables the reactive load compensation to be adaptive with the outphasing angle and, as a consequence, the output power level. The system, whose branch amplifiers are saturated class F based on matched SiGe devices, maintains a flat efficiency in excess of 50 % over a 7 dB output dynamic range. A different topology is used in [46], where an outphasing amplifier is designed at 1.95 GHz using CMOS bare devices driven in class E and combined through a coupled-line combiner. It achieves a flat maximum power around 42 dBm and a drain efficiency at 6 dB OBO higher than 60 % over a 250 MHz bandwidth. Switch-mode class E amplifiers based on GaN bare die devices are also employed in [47] with a transformer-based combiner to realise a 70-W pure outphasing amplifier at 2.3 GHz. The obtained 50% efficiency bandwidth with

CW signals is of 260 MHz at 6 dB and of 160 MHz at 8 dB back-off, respectively. Modulated measurements using a single-carrier 9.6 dB PAPR W-CDMA signal at 2.3 GHz result in drain and total efficiency of 53.5% and 43.8%. Finally, a design based on an embedding model [48] for the GaN device parasitics is presented in [49]. The outphasing PA, whose topology is the commonly employed Wilkinson combiner complemented with stub compensation elements, achieves 43 dBm peak power and 55 % PAE at 8 dB OBO at 2 GHz. An average drain efficiency of 50 % is demonstrated with a 5 MHz 9.3 dB PAPR W-CDMA signal.

The most common approach in the recent outphasing systems mentioned above is to derive the branch PA driving signals, which are both amplitude- and phase-modulated in the most general scenario, from the modulated RF input signal. This is done, for example, by extracting this information from lookup tables containing the measured performance of the system under a wide range of operating conditions. Then, digital signal processing is used to generate such branch signals from the input signal, thus requiring multiple baseband-to-RF upconversion paths. This inability to operate directly on a modulated RF input signal, however, represents a major limitation of outphasing systems that has made them less attractive than the Doherty approach in terms of complexity, cost, and power consumption [50]. Several different strategies have been proposed to decompose the input signal into the required branch drives. In [51] the decomposition is performed in the analog baseband domain, whereas other analog solutions operate at IF in a feedback configuration [52, 53], or in open-loop [54]. In 2015, Barton and Perreault [50] proposed a method to performing the signal decomposition in the analog RF domain instead of the digital domain, thus allowing to decouple the design of the baseband digital and RF analog elements, in an attempt to reduce system complexity. Additionally, this approach allows to treat the resulting single RF-input outphasing PA to be treated as a "black box" macro-PA to employ as a building block in more complex designs. In the following years, there have been successful attempts to realise RF-input outphasing amplifiers, at least narrowband. The 2.17 GHz PA in [28], based on LDMOS devices, demonstrates an average efficiency around 50 % and 45 % for 20 MHz modulated signals with 6 and 7.5 dB PAPR, respectively. The authors in [29] also present an outphasing PA in the same frequency band. It exceeds 60 % efficiency at 5.5 dB OBO at 2.14 GHz.

2.2 Bandwidth limitation analysis

The work presented in this chapter focuses on the more widespread dual RF-input outphasing, whose back-off efficiency bandwidth capabilities are assessed by identifying the possible limiting factors and isolating their individual contribution to the overall performance.

The block diagram in Fig. 2.5 helps in underlining the several factors that

have an impact on the bandwidth of a Chireix outphasing system. First of all, an essential element in any load modulated PA is the non-isolating power combiner. In addition, the working principle of the Chireix PA is based on the shunt reactive elements placed on each branch, which perfectly compensate the reactive part of the impedance seen by the branch amplifiers only at a single frequency, even if the power combiner were frequency independent. Furthermore, the device parasitics are ever-present and make the behaviour of the real device different from that of an ideal current or voltage source, as considered in the ideal analysis. It is therefore essential to understand how and to what extent each of these elements affects the bandwidth of the resulting system, in order to select the type of combiner, the realisation of the shunt reactive elements and the parasitics compensation network for the appropriate trade-off of complexity and performance.

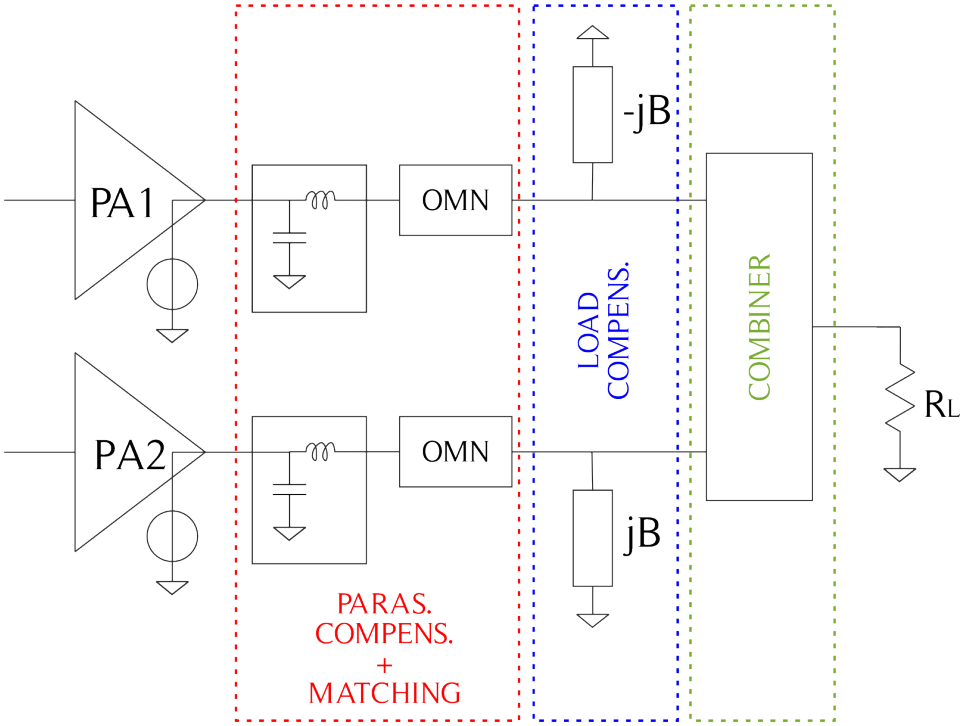


Figure 2.5: Block diagram of the output section of a Chireix outphasing system.

The design targets an output power in excess of 20 W at 3.5 GHz, which is compatible with the requirements of base stations for LTE operation. The standard assumes a OFDM modulated signal, with a bandwidth or around 20 MHz. The design is thus focused on optimising the efficiency at 7 dB back-off, consistent with the PAPR of these signals. According to the specifications, an appropriate choice of active device is the CGH40010F GaN HEMT manufactured by Wolfspeed Inc. [55], a packaged device that can deliver over 10 W peak output power at 28 V drain supply and supports operation from DC to 6 GHz. The electrical characteristics

of the selcted device are listed in Table 2.1. The PA is to be realized in hybrid IC technology on a Duroid 5880 substrate, with 0.79 mm thickness and 2.2 relative dielectric constant.

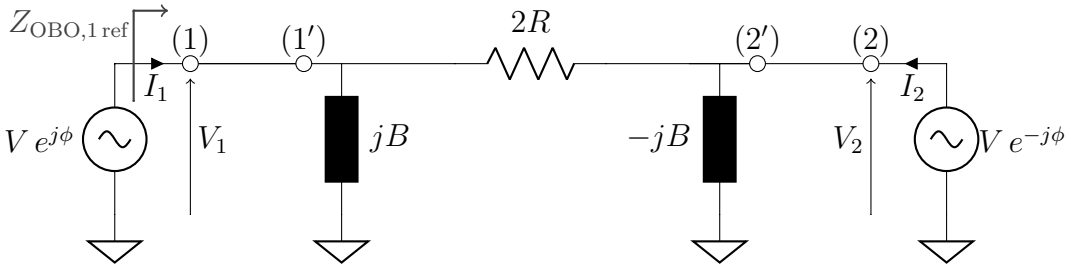
Table 2.1: Electrical characteristics of the Wolfspeed CGH40010F at 25°C.

Parameter	Description	Unit	Value
$V_{GS,th}$	Gate threshold voltage (typ. value at $V_{DS} = 10\,V$, $I_D = 3.6\,mA$)	V	-3.0
$V_{GS,Q}$	Gate quiescent voltage (typ. value at $V_{DS} = 28\,V$, $I_D = 200\,mA$)	V	-2.7
I_{DS}	Saturated drain current density (typ. value at $V_{DS} = 6\,V$, $V_{GS} = 2\,V$)	A	3.5
V_{BD}	Drain-source breakdown voltage (min. value at $V_{GS} = -8\,V$, $I_D = 3.6\,mA$)	V	120
G_{SS}	Small-signal gain (typ. value at $V_{DS} = 28\,V$, $I_D = 200\,mA$, 3.7 GHz)	dB	14.5
P_{sat}	Power output (typ. value at $V_{DS} = 28\,V$, $I_D = 200\,mA$, 3.7 GHz)	W	12.5
η	Drain efficiency (typ. value at $V_{DS} = 28\,V$, $I_D = 200\,mA$ at P_{sat}, 3.7 GHz)	%	65
C_{GS}	Input capacitance (typ. value at $V_{DS} = 28\,V$, $V_{GS} = -8\,V$, 1 MHz)	pF	4.5
C_{DS}	Output capacitance (typ. value at $V_{DS} = 28\,V$, $V_{GS} = -8\,V$, 1 MHz)	pF	1.3
C_{GD}	Feedback capacitance (typ. value at $V_{DS} = 28\,V$, $V_{GS} = -8\,V$, 1 MHz)	pF	0.2

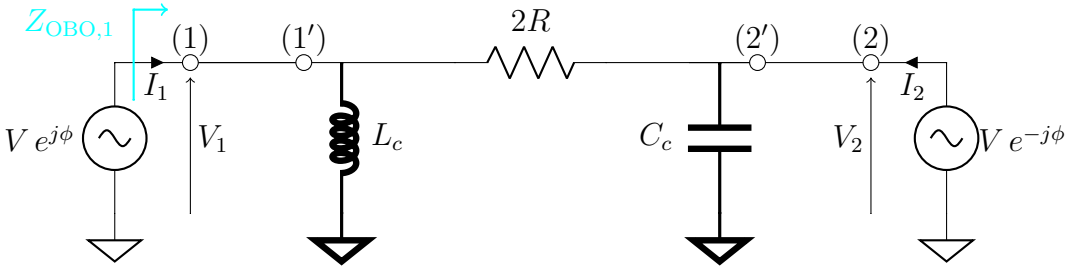
Once the active device has been selected, the following step is to choose the topology of the output section (type of power combiner, implementation of the compensation elements). As mentioned in 2.1.3, the combiner may be either a transformer, or a balun, or a $\lambda/4$ combiner, thus leading to different frequency performance away from the design frequency. The design of a balun for the targeted application is not trivial and results into infeasible parameters in a single-layer planar technology. Before resorting to more complex realizations, it is deemed necessary to assess the effect of the other components on the frequency behaviour of the overall system. A simple preliminary analysis is devised in order to assess the bandwidth limitation factors and to select the most appropriate topology accordingly.

The analysis consists of two steps. Initially, the device parasitics are neglected and the effect of combiner and compensation elements is investigated. All the cases

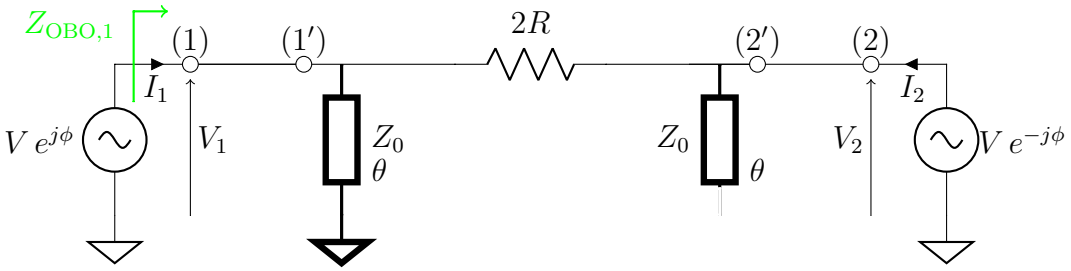
where at least one frequency dependent element is present are compared to the fully frequency independent case, shown in Fig. 2.6 (a).



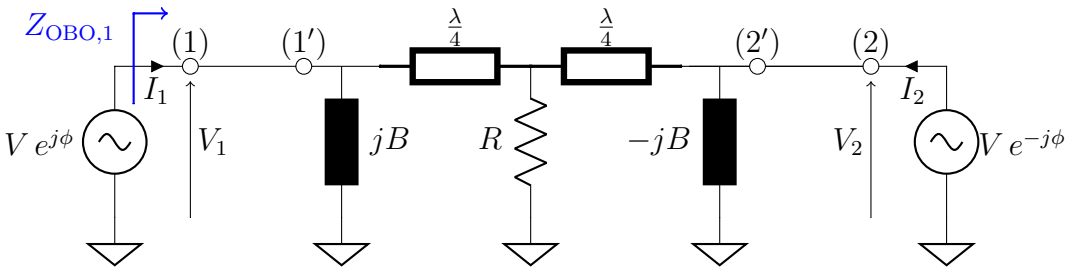
(a) frequency independent output section.



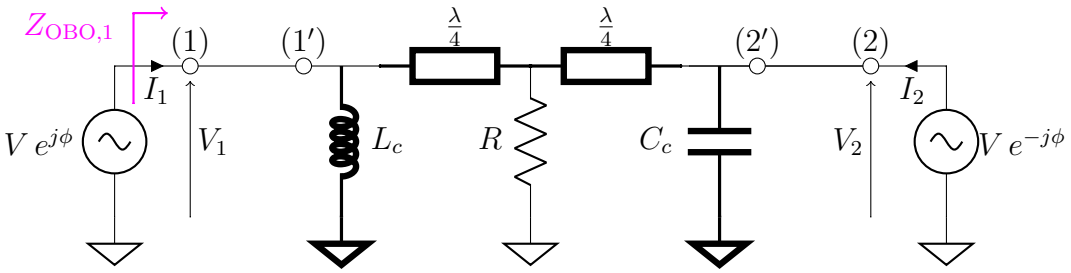
(b) frequency dependent lumped compensation elements.



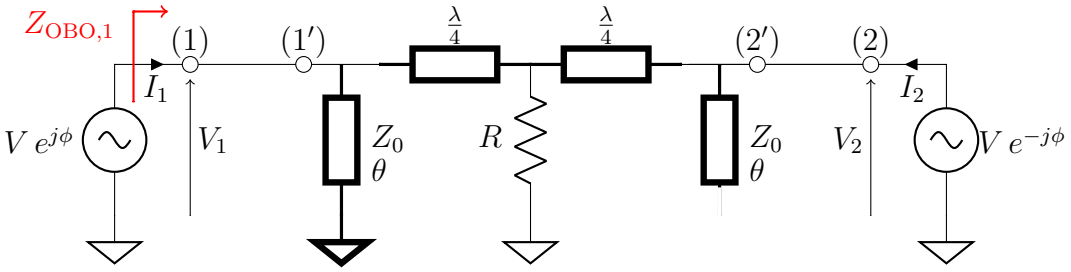
(c) frequency dependent distributed compensation elements.



(d) frequency dependent combiner.



(e) frequency dependent combiner and lumped compensation elements.



(f) frequency dependent combiner and distributed compensation elements.

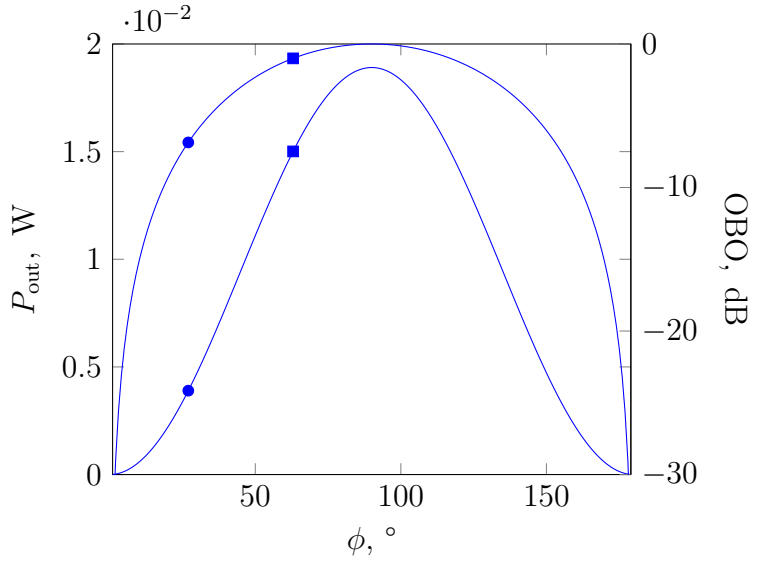
Figure 2.6: Analysed configurations of the output section.

An AC simulation is performed where the branches are driven by single-tone voltage sources with constant amplitude V and opposite variable phase $\pm\phi$. These are assumed to be the output voltages of saturated class B amplifiers driven by suitably phase modulated signals. As such, given the output voltage V_{i} and the measured output current I_{i} of the i-th amplifier, the efficiency of the system is computed as

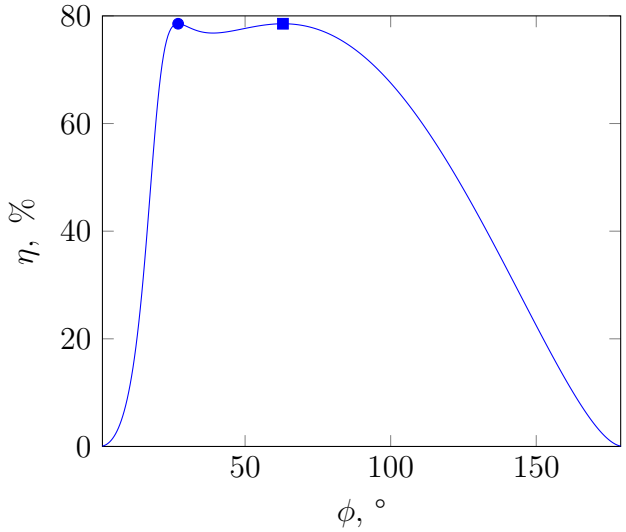
$$\eta = \frac{\frac{1}{2} V_{\mathrm{out}} I_{\mathrm{out}}^*}{|V_1|\,|I_1|\,\frac{2}{\pi} + |V_2|\,|I_2|\,\frac{2}{\pi}} \tag{2.10}$$

i.e. assuming that the voltage waveform is a sinusoid, whereas the current waveform is a half-rectified sinusoid whose peak value is that of the measured sinusoidal current I_1 (which, one should recall, is assumed to be on the tuned load). The output power is measured across the series load $2R$ in this case, where R is the optimum load resistance, and therefore $V_{\mathrm{out}} = V_1 - V_2 \equiv V_1' - V_2'$ and $I_{\mathrm{out}} = I_1 = -I_2$. The behaviour of the circuit in Fig. 2.6 (a) in terms of output power, corresponding OBO, and efficiency as a function of the outphasing angle ϕ is reported in Fig. 2.7. The corresponding load modulation trajectories are shown in Fig. 2.8 for the two branches, identified by a solid and a dashed line, respectively. The points relative to the two efficiency peaks are underlined: the square corresponds to the high power point, labelled as “peak” although it does not coincide with the peak power

point exactly, whereas the circle is the OBO point of interest. At these points each amplifier sees a purely real load and thus no reactive power is generated.



(a) output power and OBO



(b) efficiency

Figure 2.7: Performance of the ideal outphasing system.

While this ideal configuration can maintain the same behaviour at any frequency, the somewhat more realistic configurations analysed below (Fig. 2.6) will exhibit ideal behaviour at a single frequency, which is selected to be the design frequency 3.5 GHz. It should be noted that P_{out} is a normalised output power whose absolute value carries no relevant information, as it is the result of a simulation based on

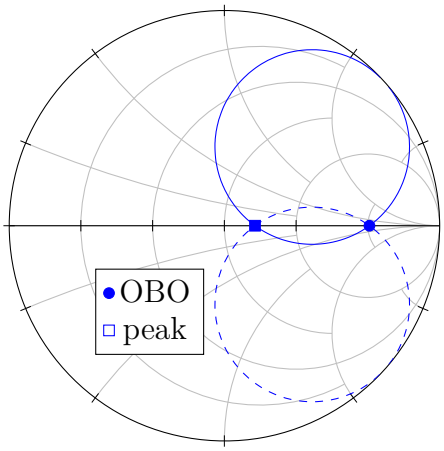


Figure 2.8: Load modulation trajectories of the ideal outphasing system.

voltage sources with normalised amplitude. The corresponding OBO is derived as $\mathrm{OBO} = P_{\mathrm{out}}|_{\mathrm{dBm}} - P_{\mathrm{out,max}}|_{\mathrm{dBm}} = 10\log_{10}(P_{\mathrm{out}}/P_{\mathrm{out,max}})$. The other considered configurations (Fig. 2.6b–2.6f) present at least one frequency dependent element, namely:

(b) the compensation elements, which are lumped (L,C);

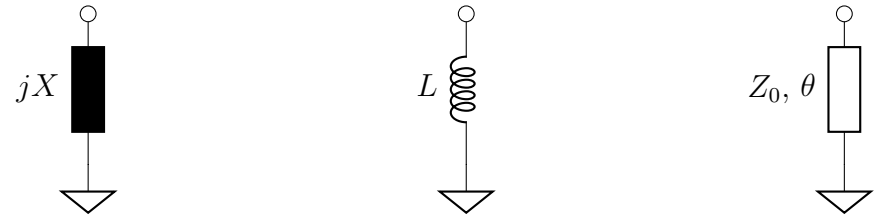
(c) the compensation elements, which are distributed (stubs);

(d) the combiner, which is made of $\lambda/4$ sections;

(e) both the combiner and the lumped compensation elements;

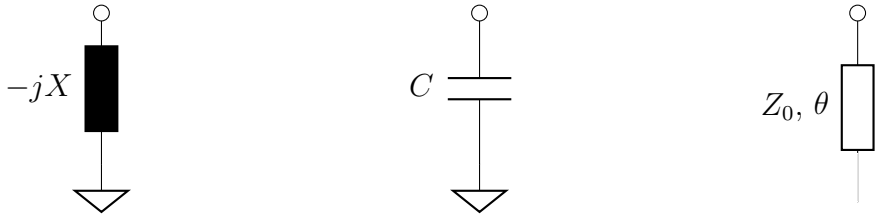
(f) both the combiner and the distributed compensation elements.

The values of L, C and the parameters (Z_0, θ) of the stubs are evaluated using the following conversion formulas in Fig. 2.9. The effect of frequency dispersion on the load modulation mechanism can be appreciated by visualizing the impedance trajectories on the Smith Chart, as shown in Fig. 2.10, which refers to the configuration in Fig. 2.6 (b). The points corresponding to the two efficiency peaks are marked using the convention introduced above. Each full circle corresponds to a full 0°–180° rotation of the outphasing angle ϕ at a given frequency, while different circles correspond to different frequencies. The same trace colour is associated to



$Z = jX$ $\quad Z = j\omega L$ $\quad Z = jZ_0 \tan(\theta),\ \theta < 90°$

(a) inductive



$Z = -jX$ $\quad Z = 1/j\omega C$ $\quad Z = jZ_0 \cot(\theta),\ \theta < 90°$

(b) capacitive

Figure 2.9: Equivalence of reactive elements.

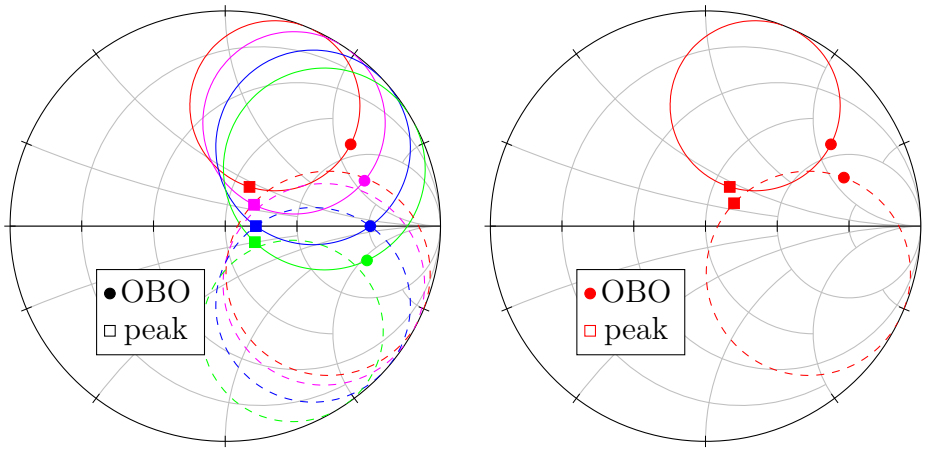


Figure 2.10: Load modulation at the voltage source planes versus frequency (left) and at a frequency lower than the centre frequency (right).

the same frequency, while the line type is representative of different branches (solid: branch 1, dashed: branch 2).

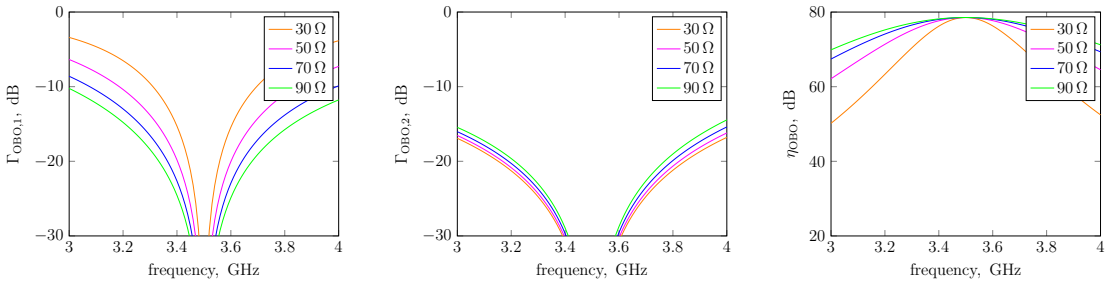
Since the target is to optimise the efficiency at 7 dB back-off on as wide a band as possible, two parameters are considered in order to give a meaningful estimation of the frequency performance: the impedance at the voltage source plane and efficiency itself. Both quantities are evaluated at the OBO level of interest, which corresponds to an outphasing angle ϕ_{OBO}. [1] The impedance at the voltage source plane $Z_{\mathrm{OBO}}(\omega)$ is referred to $Z_{\mathrm{OBO,ref}}$ of the ideal frequency independent case by defining a complex reflection coefficient

$$\Gamma_{\mathrm{OBO}}(\omega) = \frac{Z_{\mathrm{OBO}}(\omega) - Z^*_{\mathrm{OBO,ref}}}{Z_{\mathrm{OBO}}(\omega) + Z^*_{\mathrm{OBO,ref}}}. \tag{2.11}$$

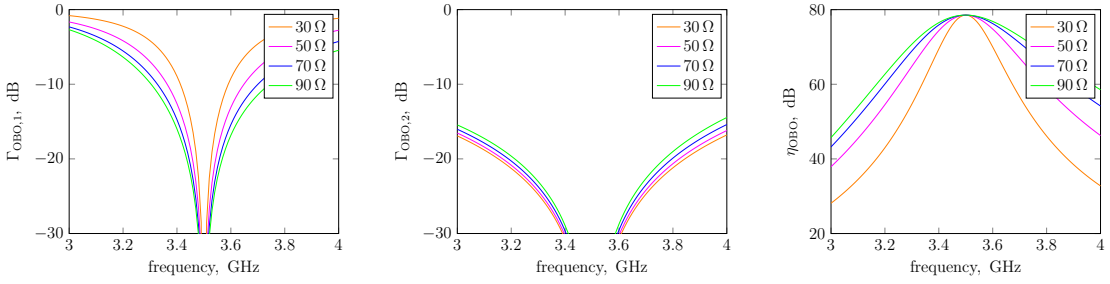
This estimates the bandwidth in that it quantifies how much $Z_{\mathrm{OBO}}(\omega)$ moves away from $Z_{\mathrm{OBO,ref}}$ by effect of the frequency dispersion present in one or more of the components (recall Fig. 2.10).

The effect of the device parasitics has initially been neglected and the device has been modelled as an ideal voltage source connected to the output section, as shown in Fig. 2.6. In this case, the intrinsic drain ports (1) and (2) coincide with the extrinsic ones (1′) and (2′), respectively. Note that, while the values of L and C equivalent to $\pm jB$ in Fig. 2.6 (b) and Fig. 2.6 (e) are unique, there are several possible implementations of the stubs in Fig. 2.6 (c) and Fig. 2.6 (f). In particular, Z_0 can be considered as a free parameter and θ is subsequently determined by the equations in Fig. 2.9. Moreover, once the required θ has been derived, any $\theta + 180°$ is also an acceptable solution. Finally, an open-ended stub of electrical length θ is equivalent to a short-ended stub of electrical length $\theta + 90°$. All these possibilities are equivalent at centre frequency, but have different frequency behaviour. Several possibilities have been analysed, varying both Z_0 and θ, together with the type of termination of the stub. They are all compared in terms of the selected figures of merit $\Gamma_{\mathrm{OBO}}(\omega)$ and $\eta_{\mathrm{OBO}}(\omega)$ in Fig. 2.11. Note that the conclusive indicator of the performance is $\eta_{\mathrm{OBO}}(\omega)$, which is a global parameter that accounts for both branches, while $\Gamma_{\mathrm{OBO,1}}$ and $\Gamma_{\mathrm{OBO,2}}$ may give contrasting or at least incomplete information if considered separately. For example, if one limited the attention to $\Gamma_{\mathrm{OBO,1}}$, one may be led to the wrong conclusions that changing the length of the stub on branch 2 has no effect, while in fact it does have an effect on $\Gamma_{\mathrm{OBO,2}}$ and therefore on the resulting η_{OBO}. In conclusion, to draw considerations on the overall bandwidth, one should consider the worst case between $\Gamma_{\mathrm{OBO,1}}$ and $\Gamma_{\mathrm{OBO,2}}$. This is the approach that has been used throughout this analysis. Fig. 2.12 summarises the results for the smallest and largest considered Z_0 in all the four configurations. It has been verified that the widest bandwidth is achieved when the stubs have the shortest electrical length (therefore, branch 1 has to be short-ended and branch 2

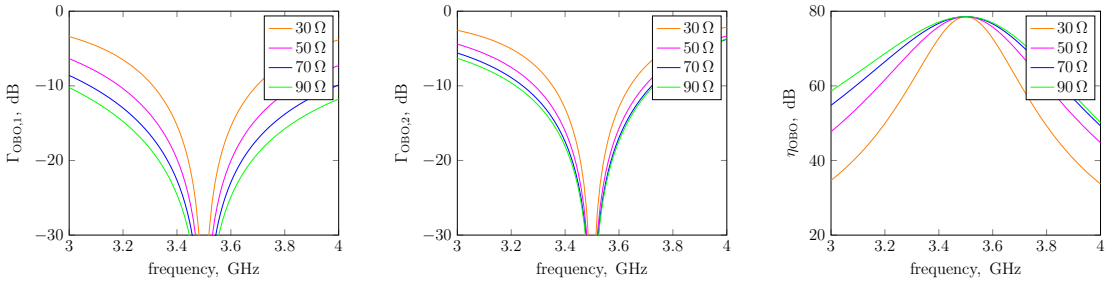
[1] Note that ϕ_{OBO} is not the same in all the configurations. When moving from the series load $2R$ to the $\lambda/4$ combiner, the point of interest becomes the complement to 90°.



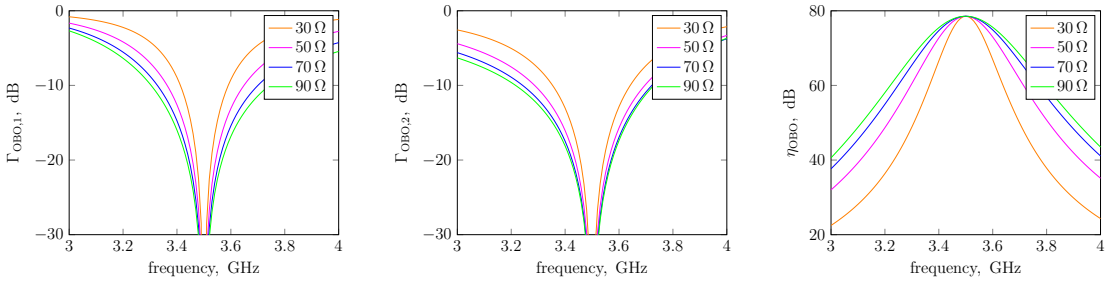
(a) 1 shorted, 2 open



(b) 1 open, 2 open



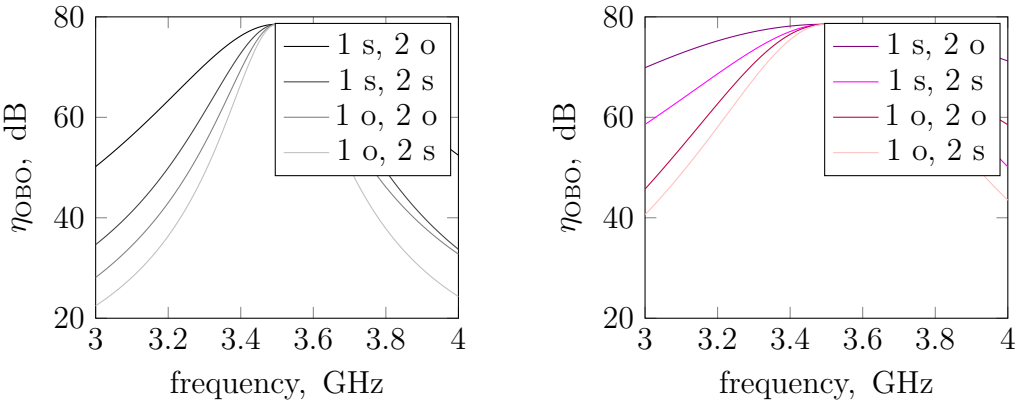
(c) 1 shorted, 2 shorted



(d) 1 open, 2 shorted

Figure 2.11: Frequency behaviour with various implementations of the distributed compensation elements.

open-ended) and the highest characteristic impedance. This has an intuitive explanation, consisting in the fact that as Z_0 increases the stubs tends to behave more and more like an ideal inductor/capacitor. This optimum configuration has been



(a) 30 Ω (b) 90 Ω

Figure 2.12: Efficiency with various implementations of the distributed compensation elements for the lowest (a) and highest (b) implemented values of Z_0.

used in the following for the comparison with the other topologies.

The comparison of all the topologies in Fig. 2.6 is drawn in Fig. 2.13. It can be observed that a combiner based on $\lambda/4$ sections poses a limitation on the bandwidth which is significantly more severe than that caused by the compensation inductor and capacitor. Therefore, when both dispersive blocks are simultaneously present, the combiner determines the maximum achievable bandwidth. If one were to make a design choice based on this first consideration, one would have to replace the simpler $\lambda/4$ with a more complex structure having wideband behaviour. However, before increasing the circuit complexity, further investigations can be made on whether the same trend is observed when the device parasitics are considered.

The simplest way to account for the drain parasitics is to add a shunt capacitance in parallel to the voltage source, thus modelling the C_{ds} of the device. This has been added between ports (1) – (1′) and (2) – (2′) of all the analysed topologies, together with an inductor L_{Cds} that compensates it completely at 3.5 GHz. In fact, to preserve the correct behaviour, one has to ensure that the load modulation that takes place at the output plane (ports (1′) and (2′)) is correctly transferred to the intrinsic drain plane (ports (1) and (2)). The fact that the compensation of C_{ds} is exact at a single frequency adds another frequency dispersion contribution which may further limit the overall bandwidth. Ideally, if an element with negative capacitance $-C_{\mathrm{ds}}$ could be synthesised, there would be no additional frequency dispersion because ports (i) – (i') would in fact coincide at all frequencies. In other words, this situation would be equivalent to the initial cases of Fig. 2.6. The chosen value $C_{\mathrm{ds}} = 1.22\,\mathrm{pF}$ is compatible with the size and technology of the employed

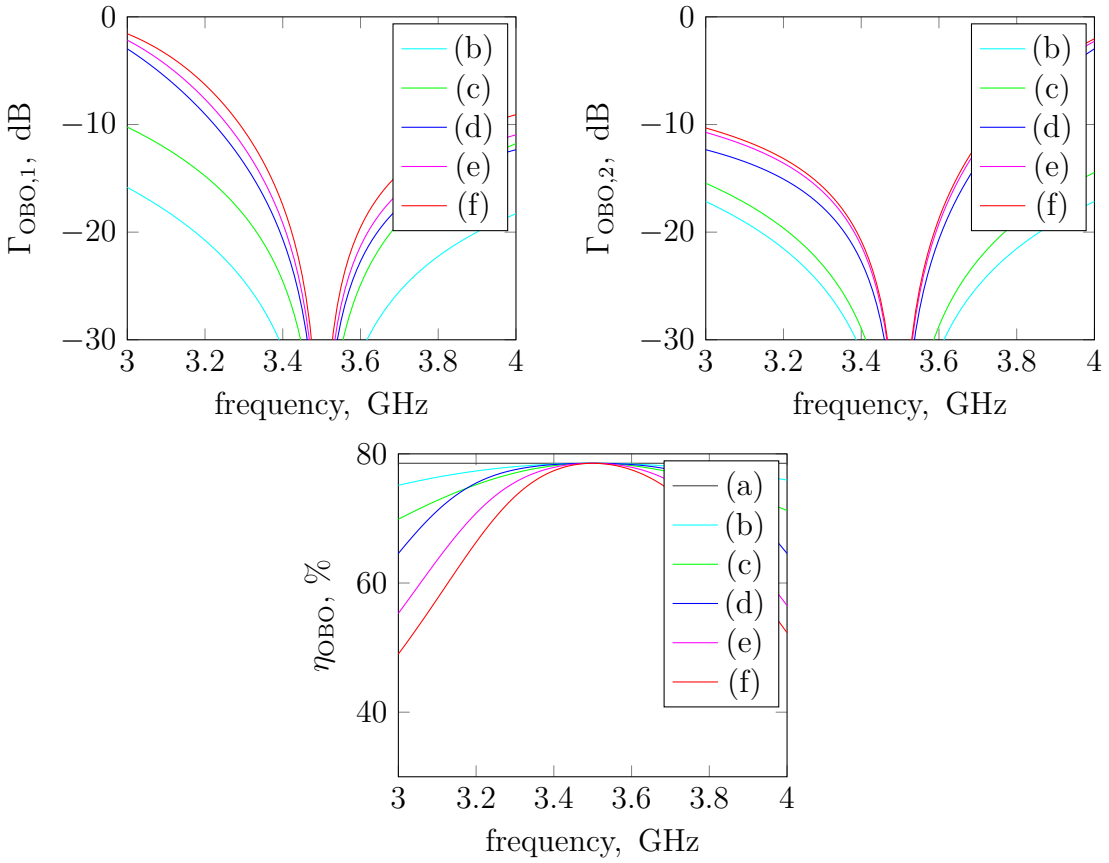


Figure 2.13: Frequency behaviour with no parasitics.

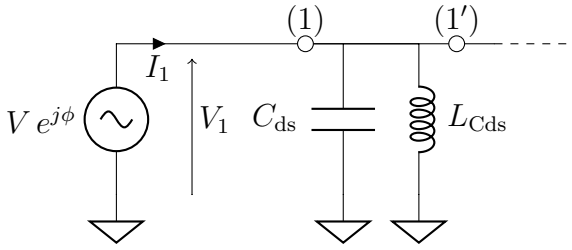


Figure 2.14: Parasitic drain-source capacitance and its compensation.

transistor. The resulting compensation inductor is derived as

$$L_{\mathrm{Cds}} = \frac{1}{(2\pi f_0)^2\, C_{\mathrm{ds}}} \tag{2.12}$$

and results to be $L_{\mathrm{Cds}} = 1.7\,\mathrm{nH}$. The frequency behaviour of all the configurations in Fig. 2.6, with the addition of C_{ds} and L_{Cds} on both branches, is reported in

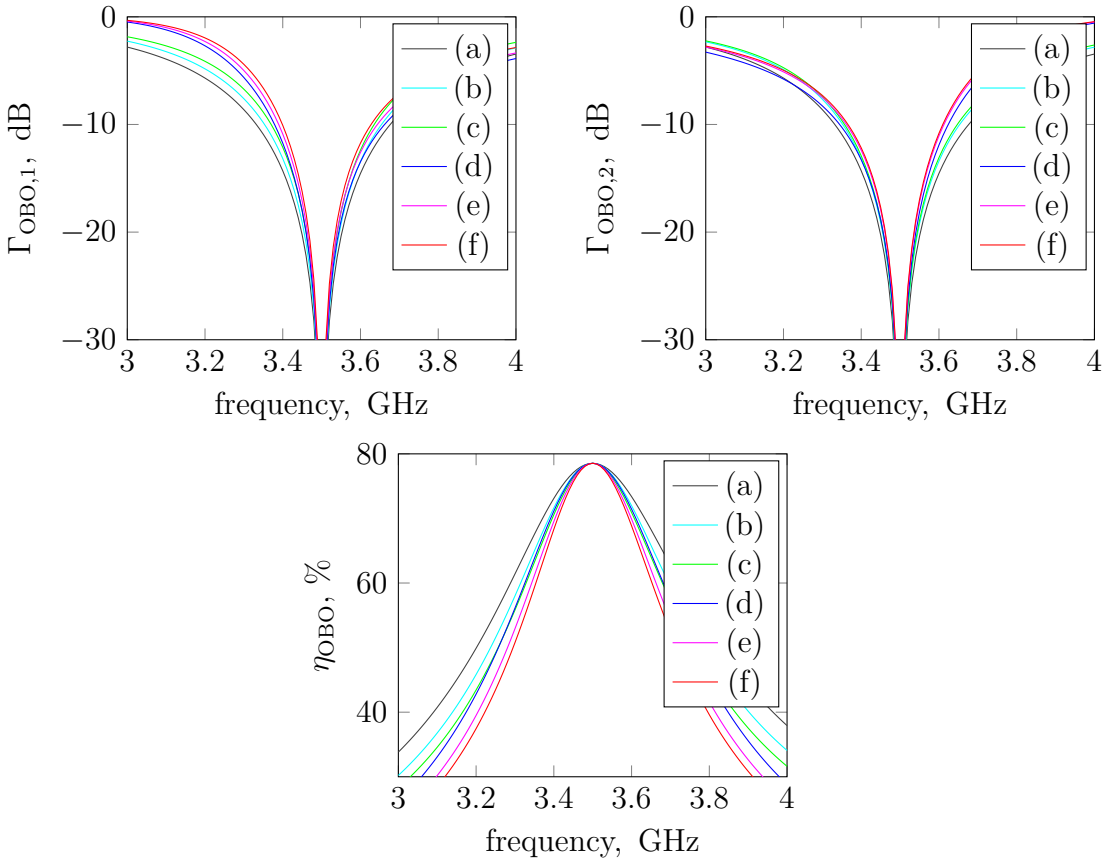


Figure 2.15: Frequency behaviour with C_{ds} compensated by L_{Cds}.

Fig. 2.15. It immediately stands out that the previous observations are no longer completely valid once the parasitics are considered. The curves are now approximately superimposed, especially if one focuses on a bandwidth of up to 500 MHz around f_0, corresponding to the -10 dB threshold. This amounts to saying that the bandwidth limitation imposed by the combiner is now comparable to that of the compensation elements, regardless of their physical implementation. What is more, considering C_{ds} is a best case, quite far from the actual condition for a packaged device like the one chosen for this design.

Before proceeding to the actual design, in which the full package model will be accounted for, an additional possibility has been considered which may bring about some advantage in case a bare die device is employed (in which case the drain parasitics are fairly represented by C_{ds} alone). It consists in absorbing C_{ds} into the shunt compensation elements $\pm jB$, either lumped or concentrated. In this case the compensation of the parasitics and of the reactive load are "merged" and carried out simultaneously by a unique element. The design formulas for the shunt elements $\pm jB_{\mathrm{extra}}$ are derived as follows. The overall susceptance B of each branch

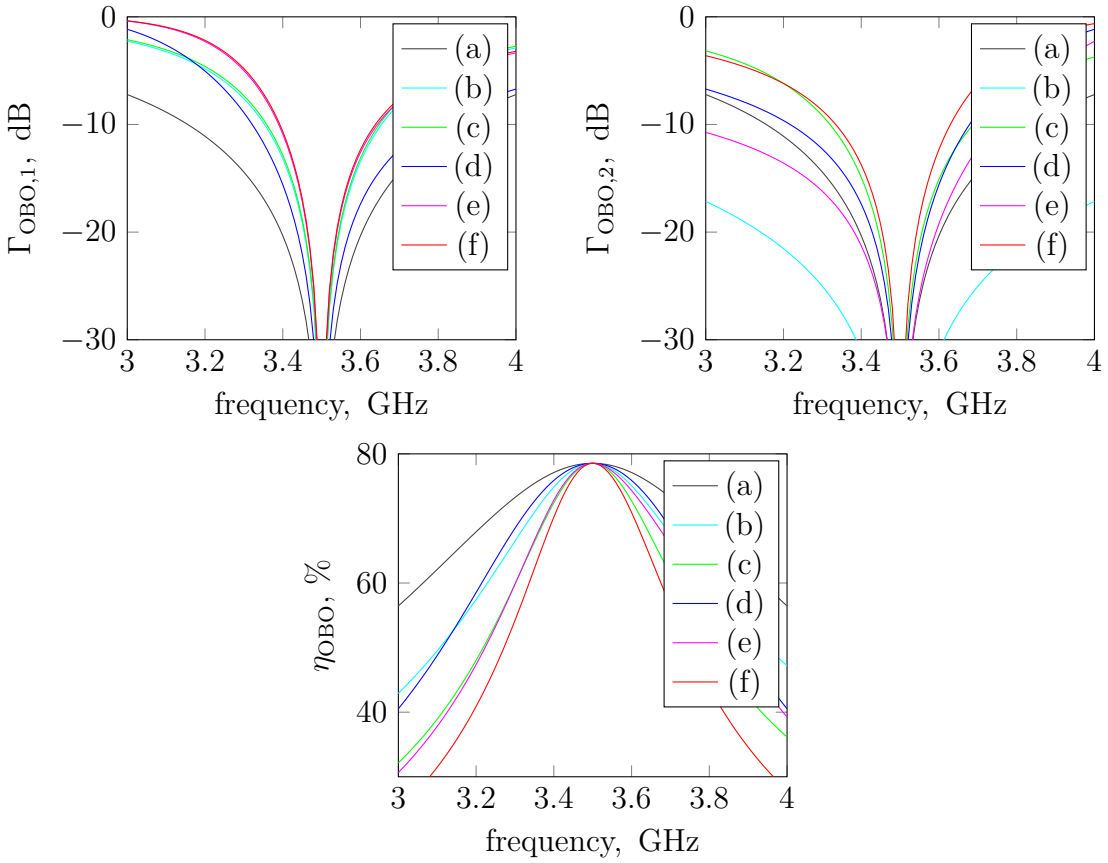


Figure 2.16: Frequency behaviour with C_{Cds} merged to the compensation elements.

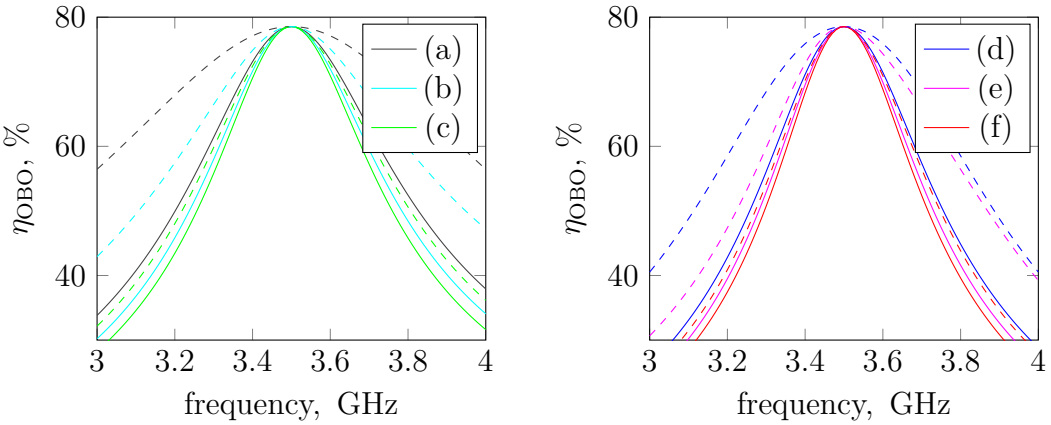


Figure 2.17: Comparison in terms of efficiency of the different ways of compensating C_{ds}.

must still be equal to the value previously found, but in this case it results from

the sum of two contributions. The first is the equivalent susceptance B_{Cds} of the drain-source capacitance, which is always positive. The second is the equivalent susceptance $B_{\mathrm{extra,i}}$ of the inductive or capacitive element added, which will be negative or positive, respectively.

$$jB_{\mathrm{Cds}} + jB_{\mathrm{extra,1}} = -jB \Longrightarrow B_{\mathrm{extra,1}} = -B - B_{\mathrm{Cds}} \tag{2.13}$$

$$jB_{\mathrm{Cds}} + jB_{\mathrm{extra,2}} = +jB \Longrightarrow B_{\mathrm{extra,2}} = +B - B_{\mathrm{Cds}} \tag{2.14}$$

These equation confirm the intuitive fact that the added elements is surely inductive in branch 1, whereas it may be either inductive or capacitive in branch 2, depending on the absolute values of B_{Cds} and B. For the considered case study, the values of B and B_{Cds} are approximately 8 mS and 27 mS, respectively. The obtained values are $B_{\mathrm{extra,1}} = -35\,\mathrm{mS}$ and $B_{\mathrm{extra,2}} = -19\,\mathrm{mS}$, therefore the shunt element to be connected to branch 2 is inductive. As a consequence, in configurations (c) and (f), such $B_{\mathrm{extra,2}}$ cannot be implemented with an open circuited stub shorter than 90°, which had been identified as the optimum choice in the previous cases. The most convenient alternative is therefore a short circuited stub on branch 2 as well as on branch 1, whose electrical lengths both result to be less than 90°. In all cases, this brings about some bandwidth enhancement with respect to keeping L_{Cds} and $\pm jB$ separated. However, the advantage is significant only if the compensation elements are ideal (cases (a) and (d)), where whereas it is much less appreciable in the other cases. This is highlighted in Fig. 2.17. The -10 dB bandwidth for either of the reflection coefficients is doubled for case (a), from 350 MHz to 700 MHz and almost so for case (d), from 280 MHz to 460 MHz. An appreciable bandwidth enhancement is also visible in case of lumped dispersive compensation elements, as long as the combiner is ideal (b). In all other cases ((c), (e), (f) the improvement is limited to few tens of MHz.

To summarise, the main observations that can be drawn from this simplified bandwidth analysis are that:

- in case of limited parasitics of active devices and passive structures, the employment of a broadband combiner may be advantageous if complemented with the absorption of the parasitic output capacitance into the load compensation network;

- a simple $\lambda/4$ combiner is suited for the selected packaged device and application, as it is not the main limiting factor of the overall bandwidth.

The goal of the design will be that of designing a suitable Output Matching Network (OMN) that compensates the device parasitics over a bandwidth as close as possible to that of the combiner itself while presenting the optimum load to the device.

2.3 Design

2.3.1 Bias point

The idealised theory of outphasing amplifiers is typically presented assuming tuned-load class B amplifiers [9], whose peak efficiency is 78.5 %. The bias point chosen during the design phase is just above the pinch-off, namely at 2.5 mA drain current, corresponding to a very deep class AB operation (well below 10 %). While the maximum achievable efficiency is slightly lower compared to class B, some linearity improvement is expected. However, the linearity of the overall outphasing architecture will be different from, although related to, that of its branch amplifiers, thus further and more detailed considerations are called for.

2.3.2 Output load compensation and matching

It has been ascertained in Section 2.2 that the transistor parasitics limit the overall bandwidth significantly. Therefore, considering them carefully and compensating for them over a sufficiently wide bandwidth is essential. Packaged transistors are affected by several other parasitic effects besides the drain-source capacitance. To carefully account for these effects, a more realistic parasitics and package model for the previously selected Wolfspeed CGH40010F device has been considered, which is reported in [56] and shown in Fig. 2.18. The values of the components are $L_1 = 0.55\,\text{nH}$, $L_2 = L_3 = 0.1\,\text{nH}$, $C_1 = 1.22\,\text{pF}$, $C_2 = C_3 = 0.25\,\text{pF}$. In particular, C_1 is equivalent to the previously considered C_{ds}. Compensating for this block is more complex than just absorbing C_{ds} into the compensation elements or resonating it out by means of an inductor. An OMN is required, which is designed in such a way as to provide a DC path for the drain supply voltage to reach the device as well as to compensate the parasitics on a sufficiently wide bandwidth. Moreover, a resistive transformation from the 50 Ω system impedance to the optimum load for power (R_{opt}) of the device is required. This task could be performed either by the OMN, or by the combiner, or by a post-matching network placed after the combiner. It was chosen to design the combiner on 50 Ω and the OMN in such a way as to perform both parasitics compensation and power matching.

Let us analyse the behaviour of the various blocks starting from the output.

The combiner is loaded by the 50 Ω system impedance and it is designed to present 50 Ω at its input ports at the maximum power condition, i.e. $\phi = 90°$ (recall 2.7). At the 7 dB back-off point, corresponding to $\phi = 117°$, the input complex impedance is $(50 \mp \text{j}104)\,\Omega$. If the imaginary part is properly compensated, the resulting input impedance will be 257 Ω. Dealing with parallel equivalent circuits and compensation elements, it is perhaps more immediate to reason in terms of admittance. The complex admittance seen at the combiner plane at 7 dB back-off is $(3.9 \pm \text{j}7.6)\,\text{mS}$, which transforms into a 3.9 mS (purely real) if the compensation

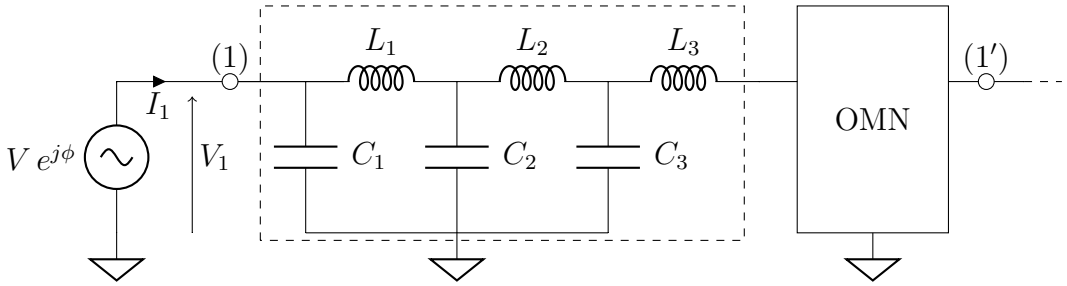


Figure 2.18: Full parasitics and package model and its compensation.

elements resonate out its imaginary part exactly. The bandwidth of the outphasing combiner is fairly simple to estimate at saturation, where the two branch signals are in phase and the excitation is thus of even type. Therefore, the simulation setup described in Fig. 2.6 reduces to a 2-port scattering simulation where the reference impedance of the input port is half of that of each branch taken separately, as shown in Fig. 2.19 (a). The resulting input reflection coefficient is reported in Fig. 2.19 (b) for the ideal TL (solid) and microstrip (dashed) implementations. On the other side, the bandwidth at the selected back-off point is of greater interest in this case, as the design aims at optimising back-off performance. At any back-off point, the outphasing combiner is driven by an "anti-symmetric" simultaneous excitation at the two input ports which cannot be reproduced by a scattering simulation. The bandwidth of the combiner in this condition is given $\Gamma_{\mathrm{OBO}}(\omega)$ defined in 2.2 of the configuration in Fig. 2.6 (d). To be exact, removing the contribution of the shunt elements $\pm \mathrm{j}B$ to frequency dispersion thus isolating the effect of the combiner alone, would require the shunt elements to cancel out the imaginary part of $Z_{\mathrm{OBO}}(\omega)$ at any frequency ω. To do so, whenever the combiner is dispersive, $\pm \mathrm{j}B(\omega)$ should be frequency dependent as well, with a law that compensated $Z_{\mathrm{OBO}}(\omega)$ exactly. This is readily reproduced in simulation and it is verified to yield a negligible difference compared to the simplest case of constant $\pm \mathrm{j}B$ implemented so far, as shown in Fig. 2.19 (c). The -20 dB bandwidth of the combiner is around 250 MHz, which fixes a goal for the design of the OMN.

As far the OMN is concerned, it should be remarked that, in case of a load modulated amplifier, an effective compensation of the parasitics amounts to ensuring the proper load modulation to be transferred from the combiner plane to the intrinsic drain. Namely, it is not enough to synthesise the desired load at saturation, as it is the case for conventional power amplifiers. A further condition, to be imposed simultaneously, is that the corresponding load at a selected back-off point is synthesised by the same network when the impedance at the combiner plane is modulated accordingly. Incidentally, this is equivalent to compensating for the parasitics and then designing a real-to-real matching network. The design is carried out with the aid of the ADS built-in optimiser, by imposing that the

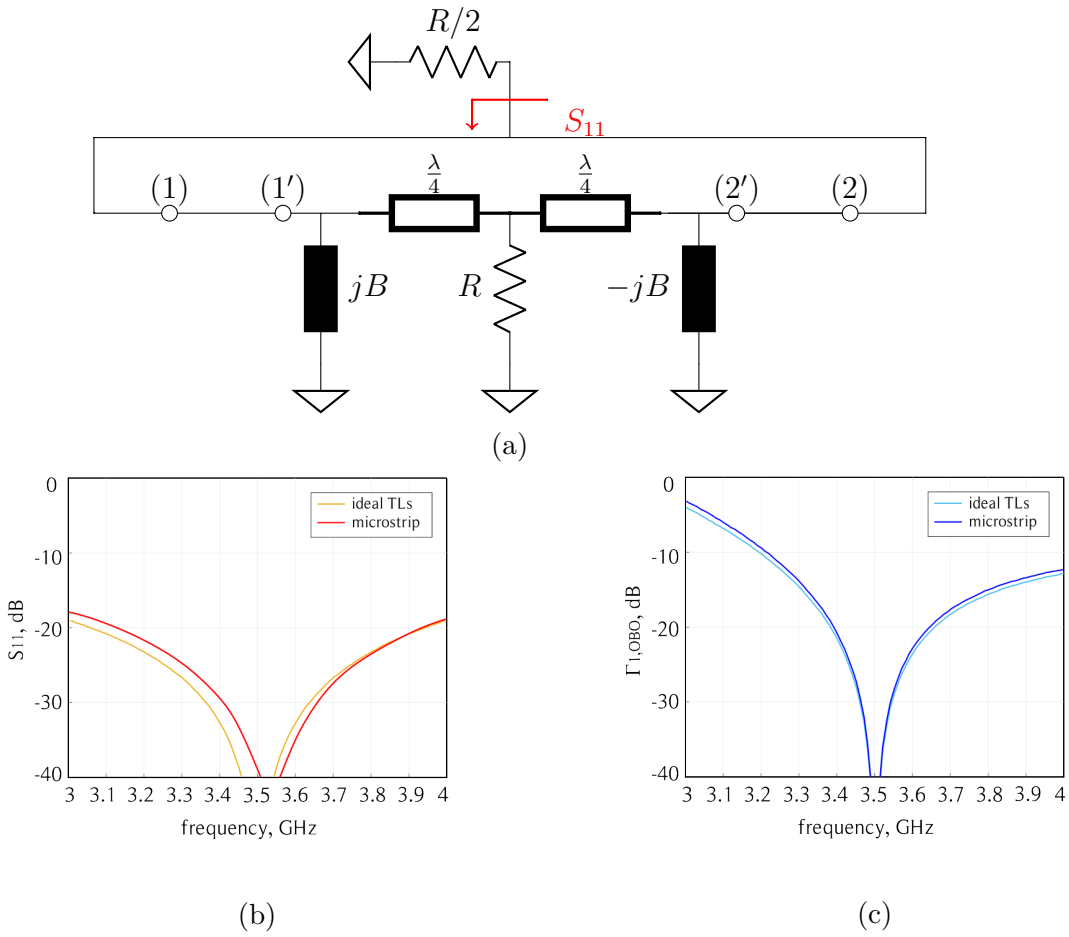
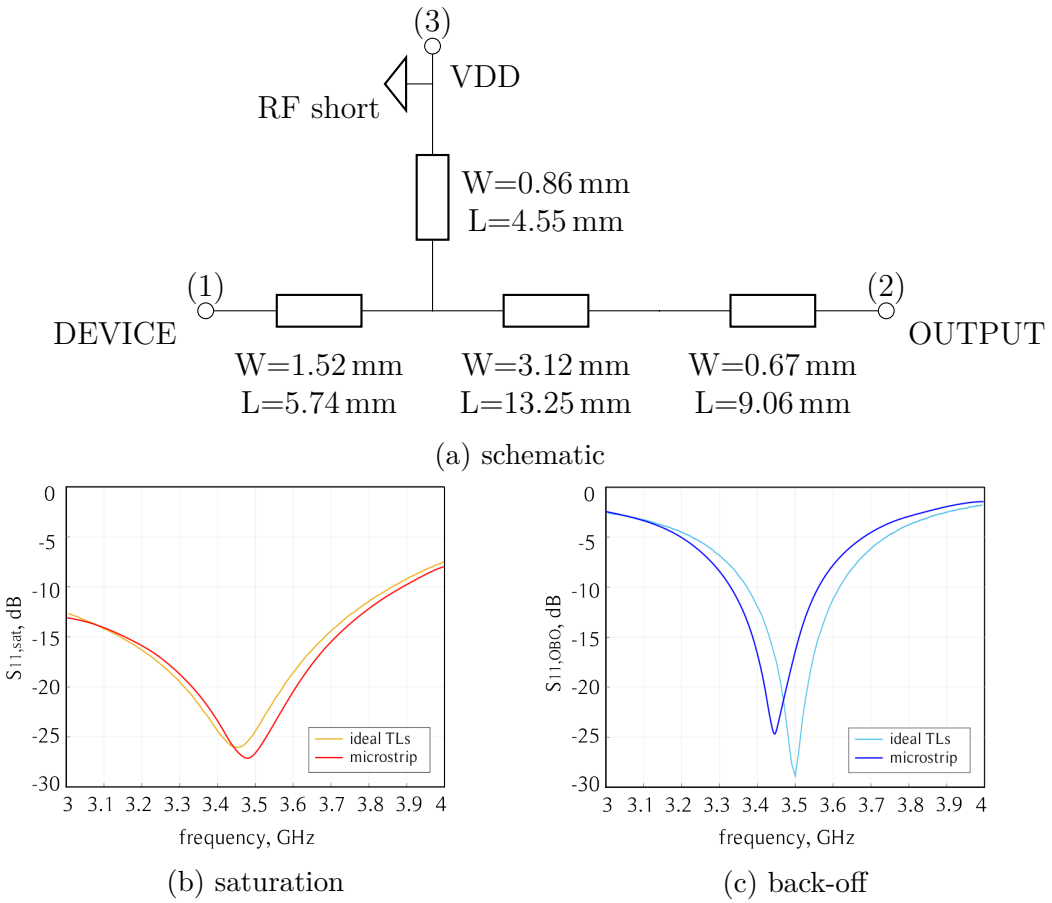


Figure 2.19: Setup for the bandwidth estimation of the combiner at saturation (a); resulting input reflection coefficient (b) and analogous in back-off (c).

impedance at the intrinsic drain terminal (port 1) is the optimum at maximum power (40 Ω) and the corresponding impedance in back-off (194 Ω) when port 2 is loaded by 50 Ω, and 257 Ω, respectively. The achieved output matching, i.e. the S_{11} of the cascade of parasitics and OMN in Fig. 2.18 computed with respect to the optimum resistance, is shown in Fig. 2.20. It can be noticed that the bandwidth achieved at saturation is larger that the back-off one. This is mostly due to the slightly larger transformation case in the latter case ($257/194 \approx 1.32$) compared to the former ($50/40 \approx 1.25$). The selected topology offers a satisfactory trade-off between achievable bandwidth and compactness. In fact, increasing the order of the filter has been verified to offer no significant improvement.

Once the design of the output section has been completed, the setup described



(a) schematic

(b) saturation

(c) back-off

Figure 2.20: Output matching at the intrinsic drain plane of the device, at saturation (b) and in back-off (c), realised by means of ideal TLs (solid) and corresponding microstrip (dashed).

in 2.2 for the preliminary bandwidth analysis has been used once more to estimate the expected performance of the overall PA. The aim is also to verify that the OMN and the combiner have indeed comparable bandwidth, i.e. than none of them is oversized, and to select the most convenient implementation of the compensating elements. The simplified voltage sources model has been used with the full parasitics model and the synthesized OMN between ports (1)–(1′) and (2)–(2′), analogously as it was done with C_{ds}. The computed $\Gamma_{\mathrm{OBO}}(\omega)$ and $\eta_{\mathrm{OBO}}(\omega)$ are reported in Fig. 2.21. It stands out that the achievable $\Gamma_{\mathrm{OBO}}(\omega)$ is comparable to the OMN back-off characteristics shown in Fig. 2.20 (c) for all the proposed configurations, thus confirming that the bottleneck to the overall frequency performance are the drain parasitics, and not the implementation of the other components. In fact, a lumped realisation of the compensation elements offers no advantage over

a distributed one. The choice of a lumped inductor on branch 1 and an open circuited stub on branch 2 is led by the ease of fine tuning rather than by bandwidth considerations.

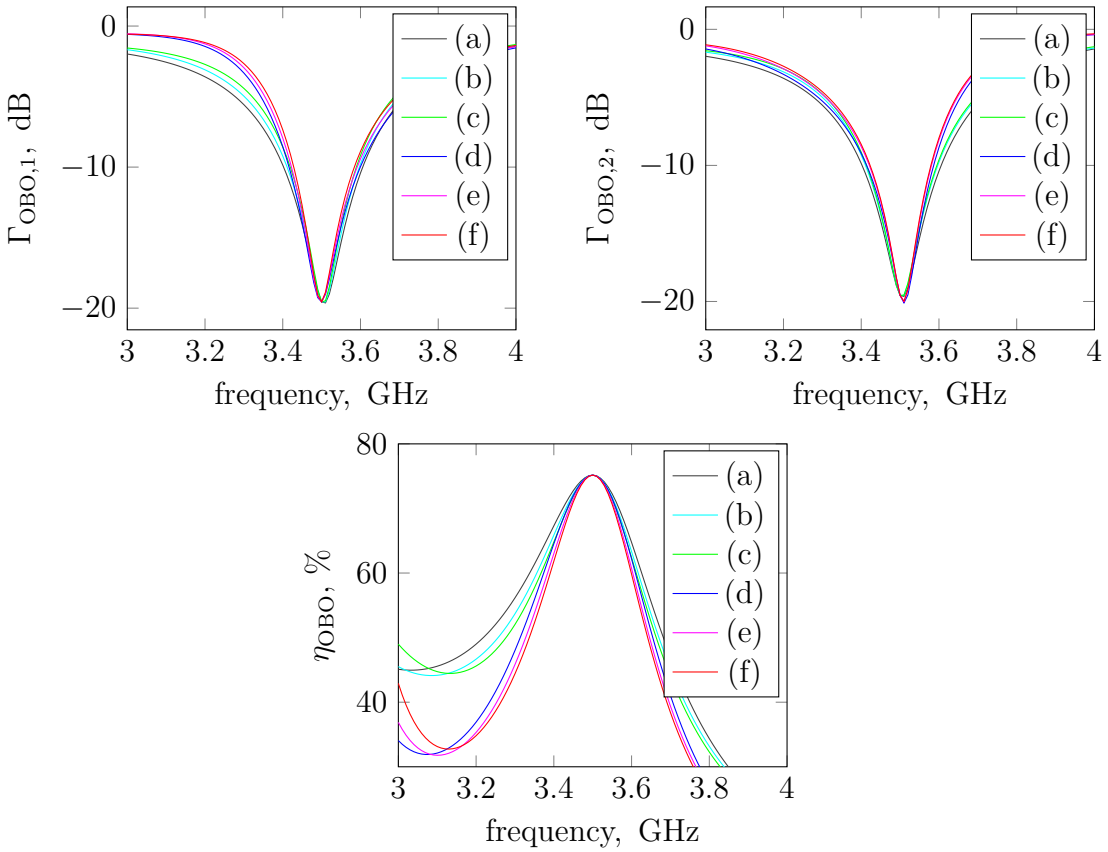
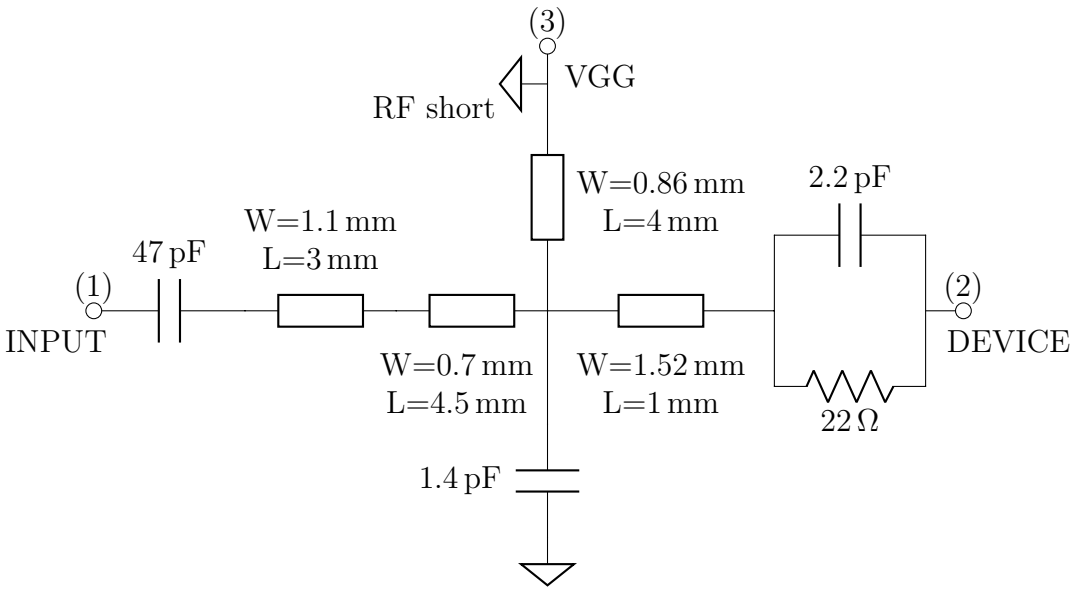


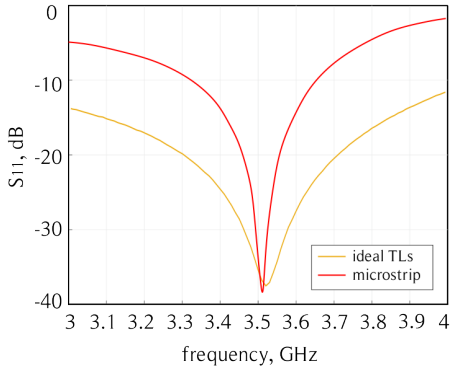
Figure 2.21: Frequency behaviour with full drain parasitics.

2.3.3 Input matching and stabilization

Finally, the design is completed by adding a parallel RC stabilisation network on the gate of each device and an Input Matching Network (IMN) chosen according to the conjugate matching criterion, to minimise input reflections. The targeted bandwidth is comparable to that achieved by the output section. The employed structure and the corresponding input matching are reported in Fig. 2.22.
The photograph of the manufactured prototype is shown in Fig. 2.23.



(a) schematic



(b)

Figure 2.22: Input matching network (a) and corresponding input reflection coefficient (b), realised by means of ideal TLs (solid) and corresponding microstrip (dashed).

2.4 Characterisation

2.4.1 Simulated performance

While the design has been performed assuming a constant-amplitude driving, as per the ideal outphasing theory, the characterisation explores a wider range of operating conditions, including input power as well as phase variations, though

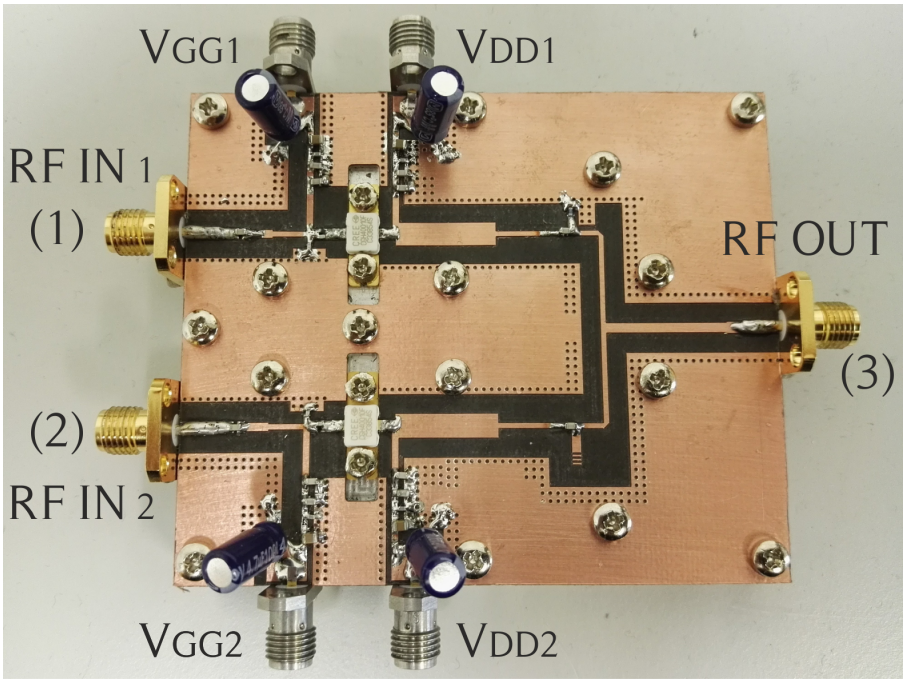


Figure 2.23: Photograph of the realized outphasing amplifier.

maintaining the phase modulation differential. This choice has a practical motivation, that is making the simulation setup as close as possible to the measurement one, where a limited amount of output power back-off can be achieved at constant (maximum) input power with the sole aid of phase variations, due to heavy stress of the active devices. In fact, especially during CW measurements, a "pure" outphasing driving would keep them in strong saturation even in deep back-off conditions. Consequently, backing-off the output power by acting on the input power as well as on the phase (what is often referred to as "mixed mode" outphasing) is expected to have a significant advantage in terms of PAE. However, in simulation, the performance of the system has been assessed in both pure and mixed mode outphasing operation, in order to estimate the advantages and drawbacks brought about by each of these method.

The first attempt refers to pure outphasing operation with an input power of 34 dBm for each branch. The frequency of the input RF signal is swept from 3 to 4 GHz with a 100 MHz spacing. The output power and corresponding OBO, as well as the overall drain efficiency and PAE of the ouphasing PAs, are plotted versus the outphasing angle ϕ for each frequency. The OBO is defined with reference to the maximum power achieved at each frequency, and the highest efficiency and PAE at 7 dB back-off are evaluated. Fig. 2.24 shows that the minimum and maximum power condition occur for ϕ around 90° and 180°, respectively, as predicted by the

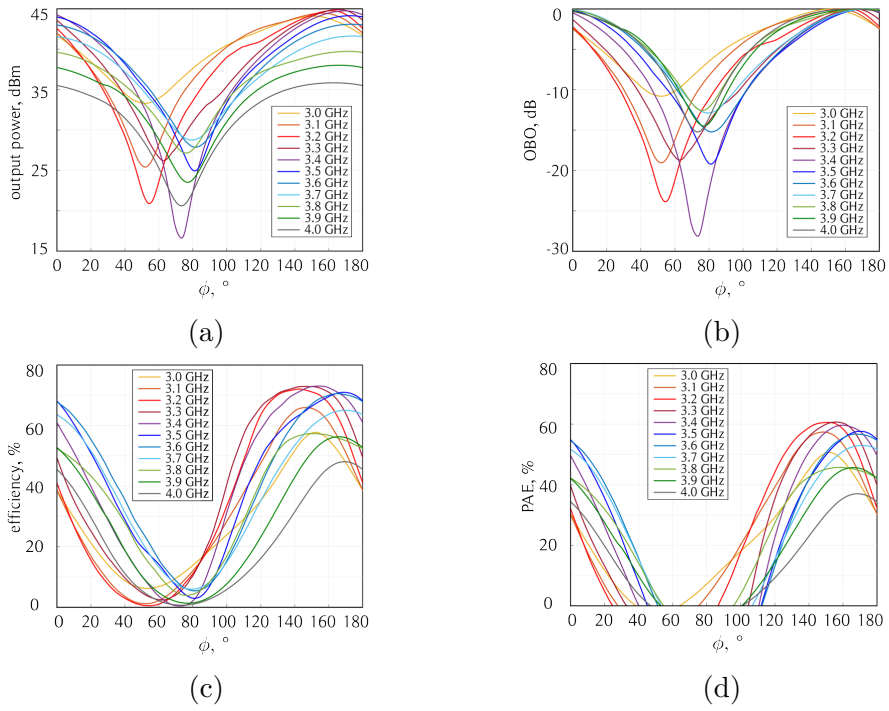


Figure 2.24: Simulated CW performance versus differential input phase.

theory. A slight shift is expected due to both frequency dispersion of the several blocks as well as tolerances of the SMD passive components and asymmetry among the two branches. For the same reason, exact power cancellation never occurs in practice. When plotted versus ϕ, the efficiency characteristics are "oval-shaped" closed curves, which have a wider aperture close to the design frequency and tend to collapse away from it. The former is indicative of a reactive load compensation that is very effective on one half of the phase domain (either $0° - 90°$ or $90° - 180°$) and completely ineffective on the other half. The latter occurs when the load modulation trajectory deviates significantly from the real axis (due to frequency dispersion), and therefore the reactive load compensation has little or no effect on the whole phase domain.

This can also be visualised on the Smith Chart by plotting the reflection coefficient (referred to $50\,\Omega$) at the intrinsic drain plane of the devices while ϕ described a full 180° rotation, as shown in Fig. 2.26. The point corresponding to 7 dB back-off is highlighted by a circle. It stands out that, although perfect cancellation of the load reactance never occurs, around the design frequency the reactance presented to each branch is reasonably low, thus leading to a good efficiency. On the contrary, at the frequency band ends, the load modulation trajectories move significantly away from their ideal position, thus making the shunt load compensation elements

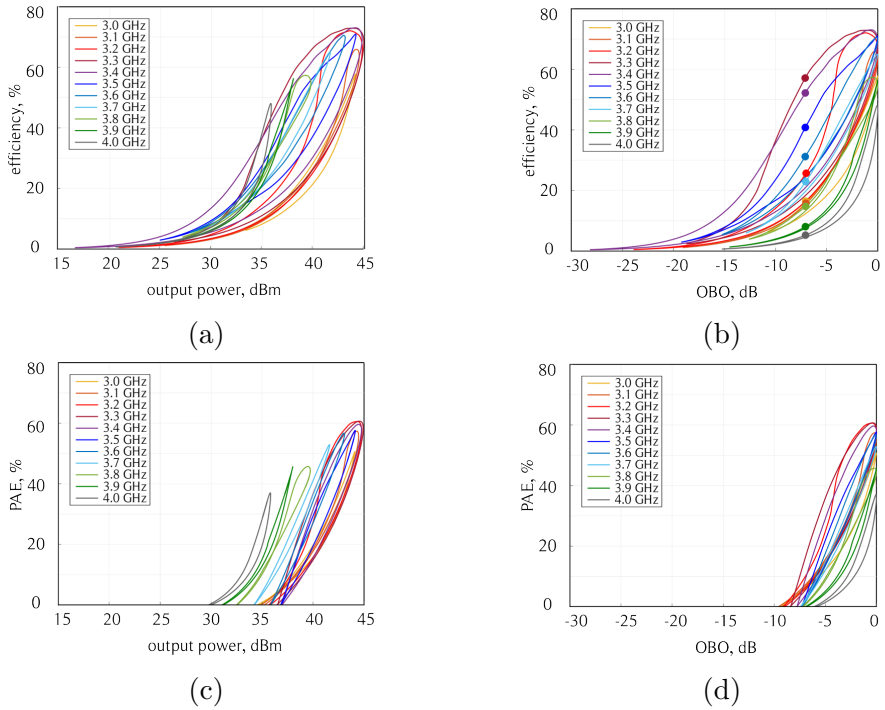
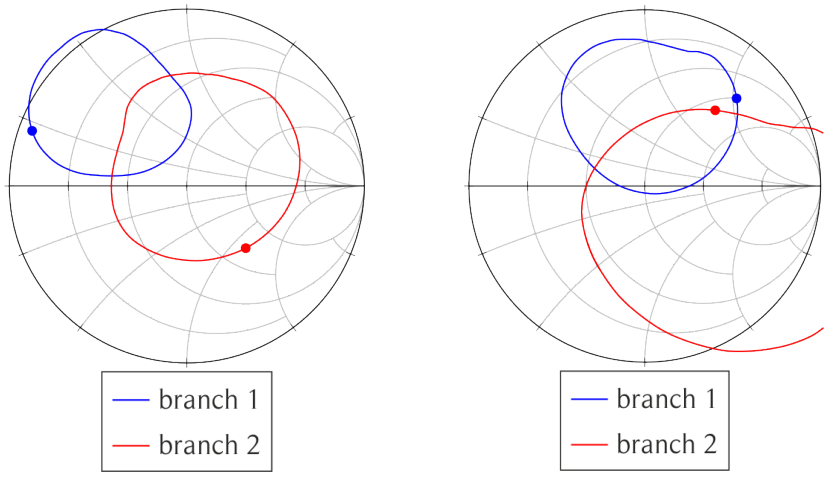


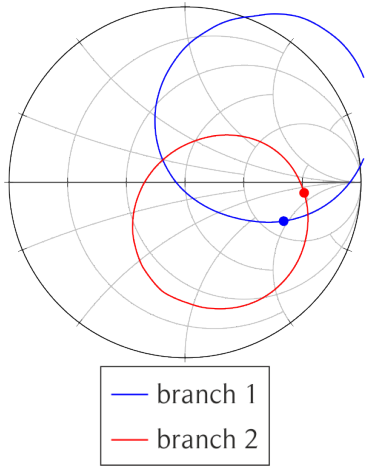
Figure 2.25: Efficiency curves versus output power (a), (c) and output power back-off (b) (d).

ineffective in cancelling out the load reactance. Fig. 2.29 (a) summarises the performance versus frequency. As previously anticipated, the PAE of the system in this operating condition is quite low, and even becomes negative as the OBO increases. In fact, 7 dB OBO is as deep as to make PAE negative in the upper end of the considered band, where the maximum power rolls off. For this reason, the subsequent analysis in two dimensions (input power and phase) and the measurement campaign explore a frequency range limited to 3.7 GHz on the high end. On the contrary, drain efficiency at 7 dB back-off is higher than 30 % on a 400 MHz bandwidth and only drops significantly above 3.7 GHz, mainly due to the power roll-off. As a consequence, the peak does not occur at the design frequency because the load compensation network has been slightly optimised to improve performance over the lower end of the frequency band. If the back-off efficiency curve is normalised with respect to its peak value and plotted versus the deviation away from the frequency f_0 at which the peak occurs, as shown in Fig. 2.30, it is possible to compare the actual performance achieved by the system (solid line) and the prediction based on the simplified bandwidth analysis (dashed lines). Only cases (e) and (f) are shown because they are the closest configurations to the actual implementation chosen for the output section. However, Fig. 2.21 clearly showed that the achievable bandwidth was approximately the same for all the considered configurations.

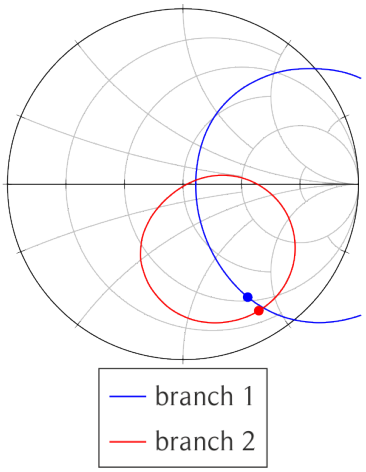


(a) 3.1 GHz

(b) 3.3 GHz



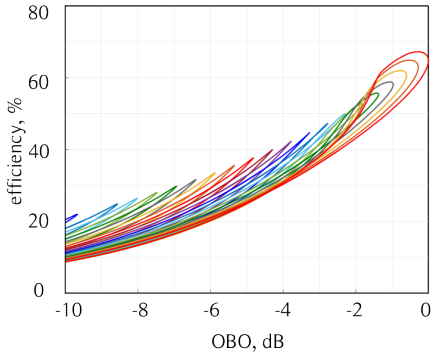
(c) 3.5 GHz

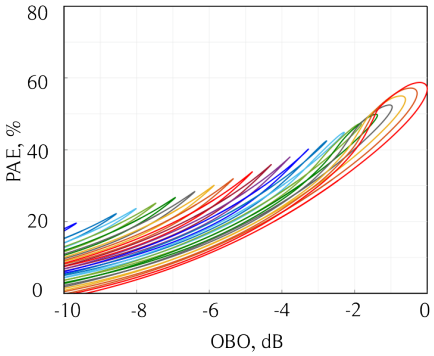


(d) 3.7 GHz

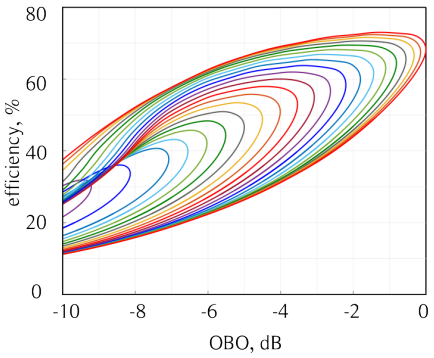
Figure 2.26: Load modulation trajectories corresponding to $P_{\text{in}} = 34$ dBm and a full 180° phase rotation.

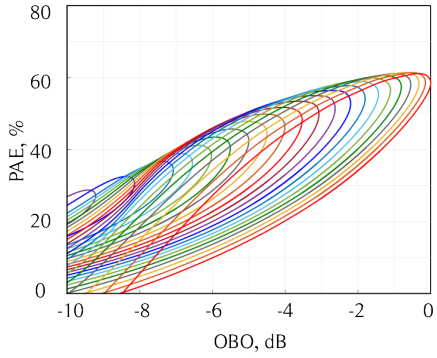
The simplified analysis predicts fairly well the 10% efficiency bandwidth, which is around 140 MHz, despite a slight asymmetry in the achieved performance.



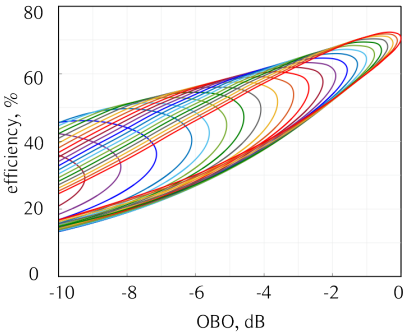


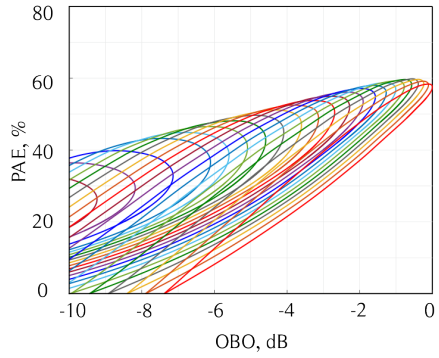
(a) 3.1 GHz



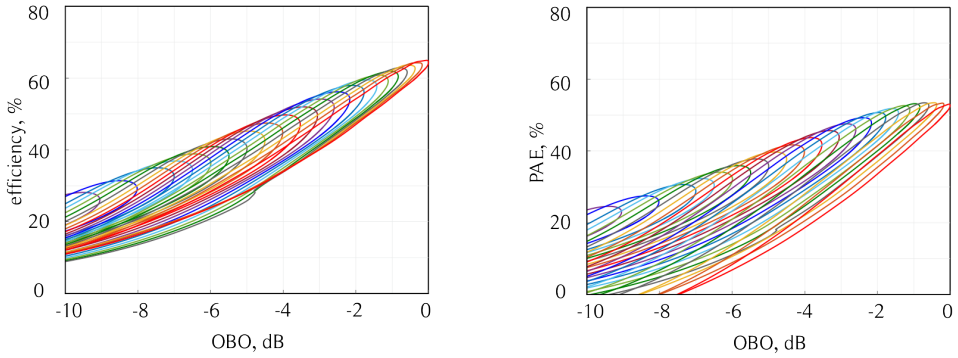


(b) 3.3 GHz





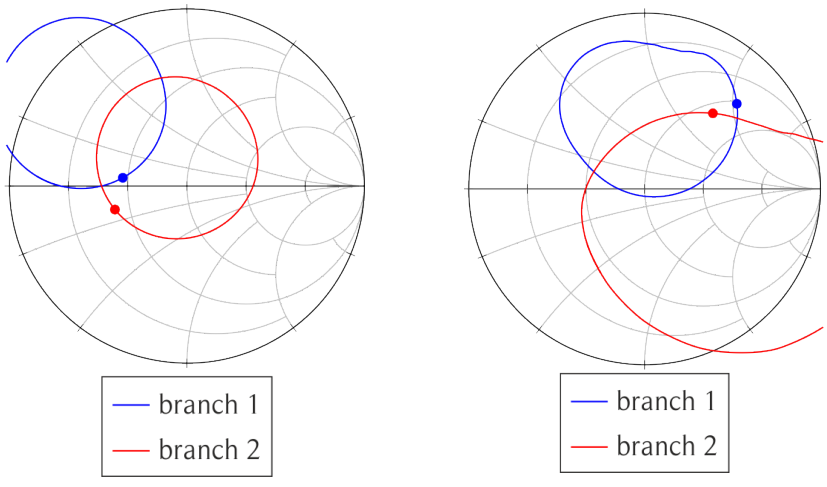
(c) 3.5 GHz



(d) 3.7 GHz

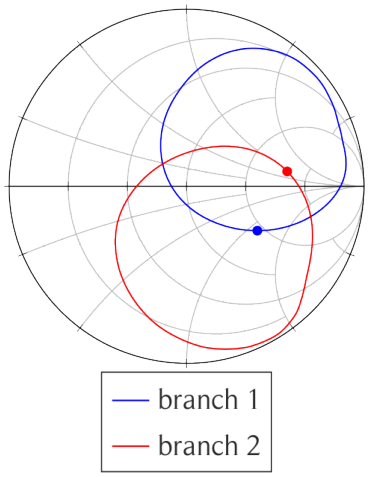
Figure 2.27: Efficiency curves versus output power back-off at selected frequencies.

As a further step, a 2D analysis is performed where input power back-off is allowed together with differential phase variations. Two nested sweeps are performed in simulation for each frequency of interest (3.1 – 3.7 GHz) and the performance of the system in each operating condition is evaluated and stored. Data post processing allows to identify all the points (P_{in}, ϕ) corresponding to 7 dB back-off from the maximum achievable power at the considered frequency and to select the one corresponding to the best efficiency or PAE, which may or may not coincide. The efficiency curves in Fig. 2.27 are analogous to those of Fig. 2.25, with the exception that each frequency now corresponds to a family of curves (one per each input power step) rather than a unique curve. Each plot reports the curves described for a full 180° phase rotation when the input power is stepped from 24 to 34 dBm. The load modulation trajectories at the intrinsic drain planes are reported in Fig. 2.28. Given the 2D nature of the present analysis, several curves would exist for each frequency depending on the input power level. Similarly, as already pointed out above, several (P_{in}, ϕ) combinations correspond to a given amount of back-off from the maximum power condition. For the sake of clarity, only the curve corresponding to the value of P_{in} yielding the highest efficiency is reported. The circle highlights the value of ϕ corresponding to 7 dB back-off. A comparison between Fig. 2.26 and Fig. 2.28 shows that the relative position of the load modulation curves in the Smith Chart is roughly the same in the 1D and 2D analysis, which means that backing off the input power has a limited effect on the effectiveness of the combiner to appropriately modulate the load of each branch and of the OMN in transferring such load modulation from the combiner plane to the intrinsic drain plane. On the other side, the 7 dB back-off points are in a similar position close to the design frequency (from 3.3 to 3.5 GHz in this case), while they are located in completely different positions at frequencies far from the design one. This suggests that, when the system is operating close to the ideal outphasing condition, backing off the input power is not necessary to improve performance. On the other side, when the

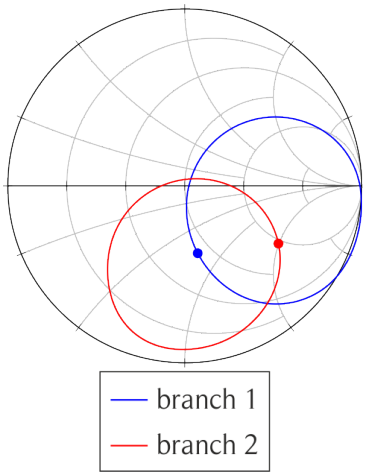


(a) 3.1 GHz

(b) 3.3 GHz



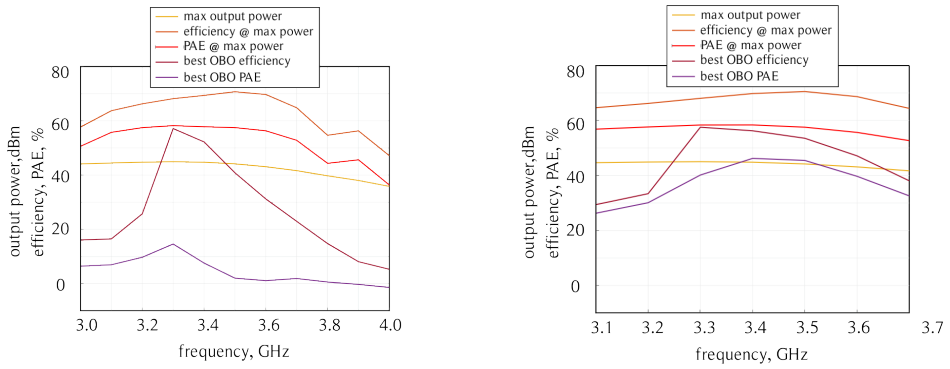
(c) 3.5 GHz



(d) 3.7 GHz

Figure 2.28: Load modulation trajectories corresponding to P_{in} driving yielding highest back-off efficiency and a full 180° phase rotation.

frequency dispersion of the several elements hampers the desired outphasing operation, backing off the input power is effective in enhancing the system performance. This observation is also supported by the highest back-off efficiency achievable in the two cases, which corresponds to the brown curve in the two plots of Fig. 2.29. In fact, the peak value, which is achieved at 3.3 GHz, is approximately the same in the two cases. Some improvement, tough limited is visible at 3.4 GHz. For all other frequencies, the "mixed mode" outphasing operation offers significantly better efficiency performance than the "pure" one. As far as PAE is concerned, as already stressed, the former is always superior to the latter, even at centre frequency. The best performance achievable by the system is summarised in Fig. 2.29 (b). The



(a) 1D (b) 2D

Figure 2.29: Simulated CW performance versus frequency for the 1D (constant input power, (a)) and 2D (variable input power, (b)) analyses.

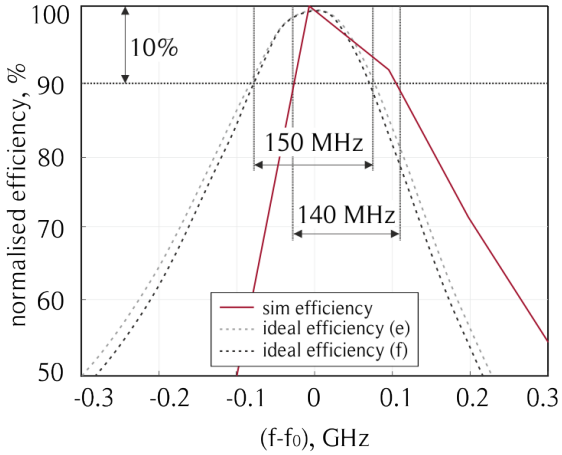


Figure 2.30: Normalised efficiency and PAE versus deviation from the peak frequency f_0.

scale of the vertical axis is purposely kept equal to the adjacent plot referring to the initial 1D analysis to ease the comparison. Of course, the performance at maximum power coincide, because the driving conditions in the two cases are the same. On the other side, back-off efficiency and especially PAE are significantly enhanced when input power is backed off.

2.4.2 Measurements

As a preliminary step before taking on the large signal characterisation, the scattering parameter of the PA are measured and compared to simulations.As there is no way of reproducing the outphasing operation in a scattering simulation, some alternative configurations are considered which may provide useful information on

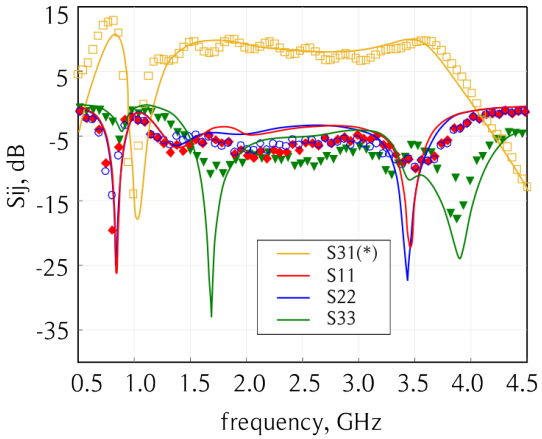
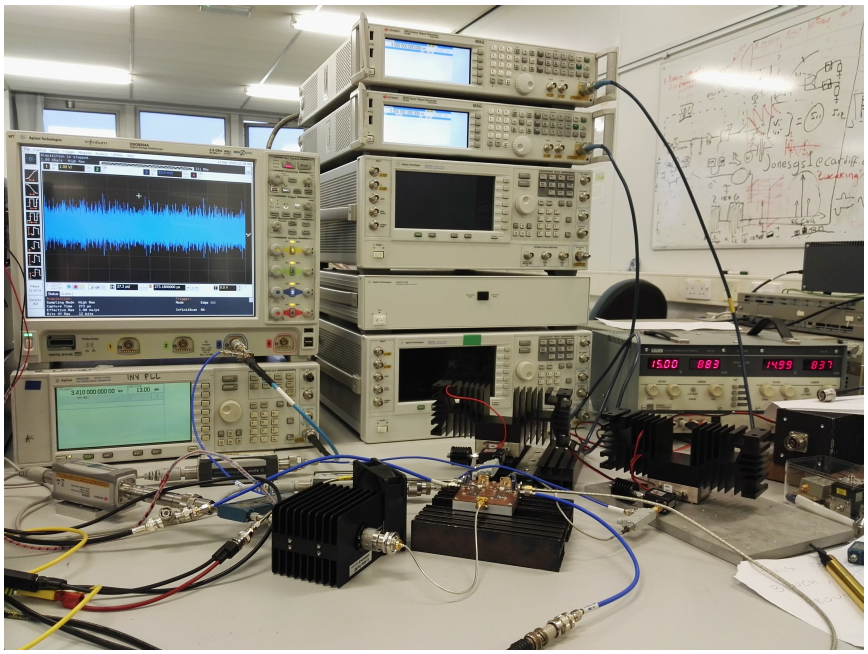


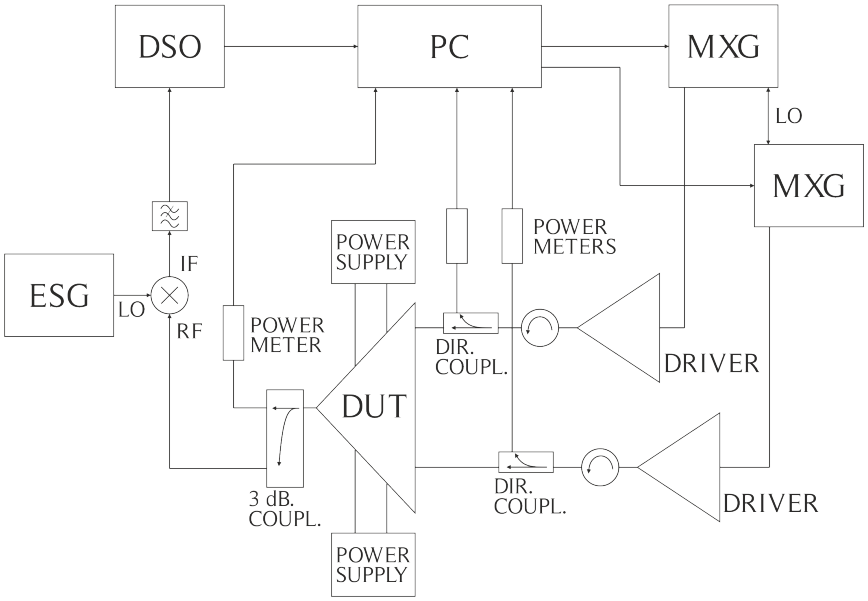
Figure 2.31: Simulated (solid) and measured (symbols) scattering parameters. (*) S_{31} refers to a configuration where the input ports are fed by a 3 dB in-phase splitter.

the proper assembly and operation of the circuit. The input matching of each branch (S_{11}, S_{22}) is evaluated while the other branch and output are terminated on 50 Ω. Similarly, the output matching (S_{33}) is assessed. Finally, a measure of the gain of the system is derived from a "balanced" configuration where the input signal is split by a 3 dB in-phase splitter and fed to each branch input, thus leading to the S_{31} curve reported in Fig. 2.31. For this measurement to be meaningful, a shallower class AB bias point is selected rather than the one used for the design, for which no small signal gain is basically visible. The selected bias is such as to provide a 45 mA DC drain current to each branch. In all cases, a satisfactory agreement between simulations and measurements is observed. After this verification, which however provides no information on the correctness of the shunt load compensation elements, one can proceed to the large signal characterisation campaign. Fine tuning of the compensation inductor and of the stub length is performed at this stage.

According to the guideline provided by the simulations, the measurement campaign has been carried out in the 3.1–3.7 GHz range. In fact, as predicted, it has been verified that the achievable output power drops below 43 dBm above 3.7 GHz. Pure outphasing operation at constant input power has been attempted initially, but after device heating and subsequent failure, it has been deemed necessary to resort to mixed mode outphasing for the complete characterisation. The employed 2D approach is completely analogous to the one that will be described in 3.3.3. Nested sweeps of P_{in} and ϕ are performed for each frequency, and the system performance in terms of output power, efficiency, PAE and is recorded at each point. All the points corresponding to 7 dB back-off from the maximum achievable power are then identified during the post processing phase and the best one for efficiency



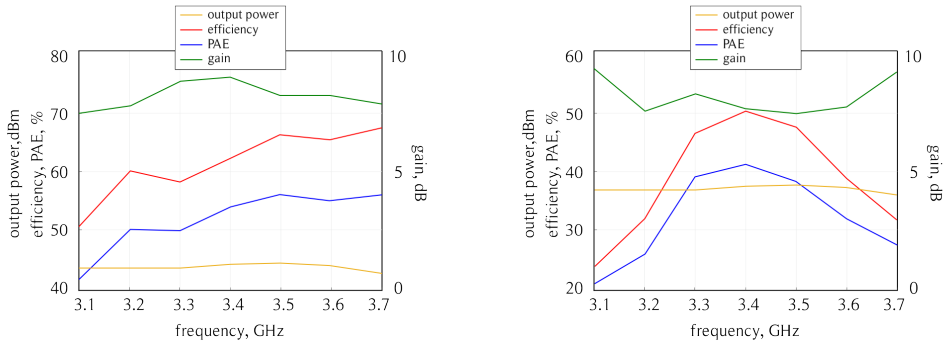
(a)



(b)

Figure 2.32: Photograph and functional scheme of the measurement setup of the Centre for High Frequency Engineering (CHFE) at Cardiff University.

is selected. Unlike in simulation, however, a full 180° phase rotation is never performed at high input power, to avoid unnecessary stress to the active device. On



(a) saturation (b) back-off

Figure 2.33: Measured CW performance versus frequency at saturation (a) and in back-off (b).

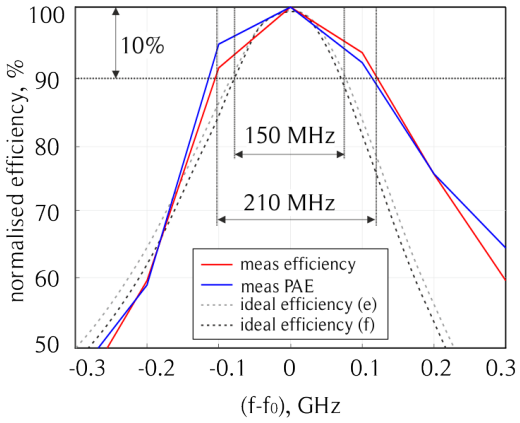


Figure 2.34: Normalised efficiency and PAE versus deviation from the peak frequency f_0.

the contrary, the ϕ values corresponding to constructive interference of the branch signals is identified during the setup calibration phase, and the measurements are only performed in such a phase range.

A photograph and the scheme of the measurement setup available at Cardiff University are shown in Fig. 2.32. The two input signals are generated using two RF vector signal generators (Keysight N5182B MXG) sharing the same local oscillator to maintain phase coherency at RF and baseband. Two nominally identical linear drivers amplify the RF signals and feed them to the DUT inputs. The input incident and reflected waves, and the output power, are measured by means of power sensors through pre-calibrated directional couplers. The demodulation chain at the output is made up by a mixer, a Keysight E4422B ESG RF signal generator used to generate the LO and a Keysight DSO9254A oscilloscope (DSO) used as a receiver to

acquire the signal performing digital I-Q down-conversion to IF. The setup natively supports modulated RF inputs, thus allowing a system level characterisation. CW measurements are performed without any hardware modification of the test bench, by simply adopting a constant baseband signal.

The measured CW performance in the 3.1–3.7 GHz range is reported in Fig. 2.33. The PA achieves the maximum saturated power at 3.5 GHz, and maintains a power in excess of 43 dBm over the whole frequency band of interest, which is consistent with the design specifications. The corresponding drain efficiency and PAE at maximum power are larger than 51% and 42%, respectively, while they are higher than 24% and 21% at 7 dB OBO. Focusing on the back-off performance, both drain and power-added efficiency have their peak at 3.4 GHz, which is fairly well predicted by simulations. Additionally, a performance within 10% of the maximum is maintained over a 200 MHz band around 3.4 GHz, which is consistent with the maximum achievable efficiency bandwidth predicted by the preliminary simplified analysis (recall Fig. 2.21). It can also be observed, both in simulations that high efficiency is maintained over a narrower bandwidth in back-off than at saturation, which is in agreement with the bandwidth of the combiner Fig. 2.19 as well as the load modulation capabilities of the OMN Fig. 2.20. Fig. 2.34 shows the normalised back-off efficiency and PAE curves (solid lines) compared to that of the simplified bandwidth analysis (dashed lines). The comparison, analogous to that presented for the simulated performance, shows a fairly good agreement between the prediction and the achieved performance. In this case, as measurements are carried out according to the "mixed mode" approach, the achieved 10% efficiency bandwidth is 210 MHz, slightly wider than the prediction based on the "pure" outphasing operation. On the other side, the measured curves show a higher symmetry with respect to the peak frequency f_0 than the simulated ones.

Chapter 3

The Doherty Power Amplifier

The Doherty power amplifier has had a significant success in recent times, both academically and commercially, for its inherent simplicity and all-RF operation. In its original formulation, it is a two-PA architecture which allows to keep the efficiency reasonably high over a wide dynamic range by exploiting the load pulling effect of the auxiliary on the main amplifier.

This chapter is organised as follows. Section 3.1 presents a simplified theoretical analysis of the conventional architecture, while the limitations that affect practical implementations are summarised in 3.2. Section 3.3 is devoted to the analysis of the dual-input topology, mainly focussing on its advantages and disadvantages compared to the single-input one. Initially, a dual-input DPA is studied in terms of optimum driving strategies and the performance improvement compared to the analogous single-input version is estimated. This analysis has led to the publication of works [57, 58], which were presented in 2018 at the International Wireless Week in Chengdu and at the European Microwave Week in Madrid, respectively. Secondly, the same dual-input DPA is used as a test structure with the aim of re-designing an improved single-input version. It is characterised with simplified driving strategies as a means of re-designing an improved input section for the single-input structure, which was initially narrowband and presented some issue. This work has been submitted for publication at the European Microwave Week which is going to be held in 2019 in Paris.

3.1 Theory

The Doherty Power Amplifier (DPA) is named after its inventor W. H. Doherty, who first proposed this architecture in 1936 [14]. Its simplified block diagram was introduced in Chapter 1 (Fig. 1.4 (a)): the *auxiliary* (or peaking) amplifier acts as an active load for the *main* (or carrier) amplifier in the high power region of operation.

In the conventional topology, the main amplifier is a class B or class AB amplifier, the latter being often preferred for its higher linearity [9]. It is designed to reach its maximum output voltage swing, and thus its maximum efficiency, at the so-called break point, which coincides with the auxiliary turn-on point. The auxiliary current is injected into the common load, where it sums to the main one thus modulating its load impedance. In the classical DPA implementation the main maximum current contributes to half of the maximum total current, which sets the break point at 6 dB OBO. The auxiliary device is off for input powers below the break point value and is turned on when input power increases above this level.

The operation can be therefore split into two different regions: the low power region where the auxiliary device is off and the Doherty region where both devices are on and load modulation occurs. Fig. 3.1 outlines the output section of a DPA in the two operating regions in its simplified form, where active devices in common-source configuration are well approximated by controlled current sources up to saturation and their parasitics are neglected.

In the low power region (Fig. 3.1 (a)), only the main device is contributing to the output power, while the auxiliary device present an open circuit to the common node. The efficiency increases with power as for a standard class AB PA, as shown by the red curve in Fig. 3.2. At the break point, the main device drain voltage reaches its maximum swing and cannot increase any further, and the auxiliary turns on.

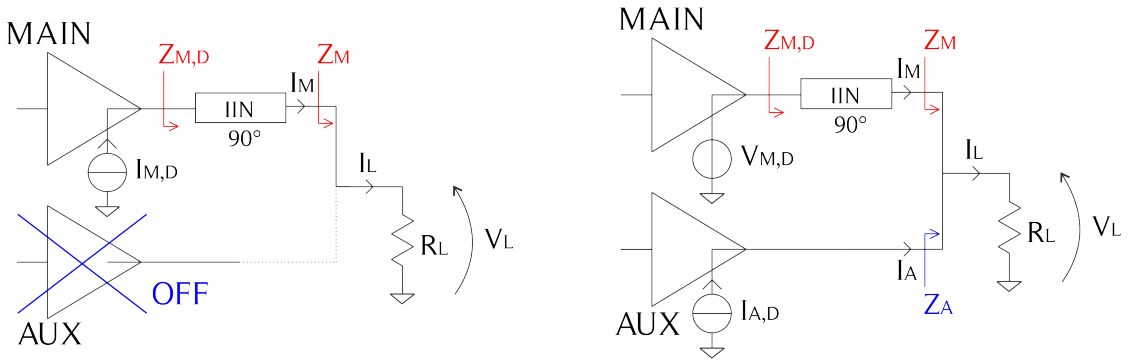
In the Doherty region (Fig. 3.1 (b)), both PAs contribute to the output power. The impedance seen from each branch is modulated by the current contribution of the other:

$$Z_{\mathrm{M}} = R_{\mathrm{L}}\left(1 + \frac{I_{\mathrm{A}}}{I_{\mathrm{M}}}\right) \qquad \text{and} \qquad Z_{\mathrm{A}} = R_{\mathrm{L}}\left(1 + \frac{I_{\mathrm{M}}}{I_{\mathrm{A}}}\right)$$

Note that I_{M} and I_{A} are complex phasors. If their relative phase is set appropriately (by the input section), Z_{M} varies from R_{L} (low-power region) to $2R_{\mathrm{L}}$ (saturation), while Z_{A} goes from an open circuit to $2R_{\mathrm{L}}$, where $R_{\mathrm{L}} = R_{\mathrm{opt}}/2$, R_{opt} being the optimum load of the class AB PA. Indeed, a decrease of its load impedance is needed to keep the main device working at maximum efficiency; therefore, on the main branch, an Impedance Inverting Network (IIN), which is typically a quarter-wavelength line, must be added to ensure the desired load modulation. The IIN transforms an impedance Z_x at one end to an impedance proportional to $1/Z_x$ at the other end. As a consequence, the increase of Z_{M} due to I_{A} is transformed into a decrease of the impedance Z_{MD} seen at the main drain plane, which results in a constant V_{MD} in the Doherty region (hence the voltage source representation in Fig. 3.1 (b)) and consequently maximum efficiency in the Doherty region. In the Doherty region, the auxiliary amplifier also contributes to the output power, with an efficiency that increases with power as shown by the blue curve on Fig. 3.2. At maximum power, both amplifiers operate at their maximum efficiency and they contribute equally to the output power, which is therefore 6 dB higher than that

at the break point (a 3 dB contribution coming from each branch). The black curve corresponds to the system efficiency resulting from the main (red) and auxiliary (blue) contributions, assuming that the two devices have the same maximum efficiency, which serves as a normalisation factor in the plot. The DPA has two efficiency peaks, one at the break point and the other at saturation, and it maintains a relatively high efficiency in the whole Doherty region.

Note that the IIN introduces a 90° phase difference, which must be compensated for in order to maintain the proper phase relation between I_M and I_A and sum them constructively at the output. This is typically achieved either by means of a 90° delay line at the input of the auxiliary amplifier or adopting an input power splitter that embeds a 90° phase shift of its output signals, such as 90° hybrid coupler.



(a) Low-power region.

(b) Doherty region.

Figure 3.1: Simplified equivalent output section of a DPA.

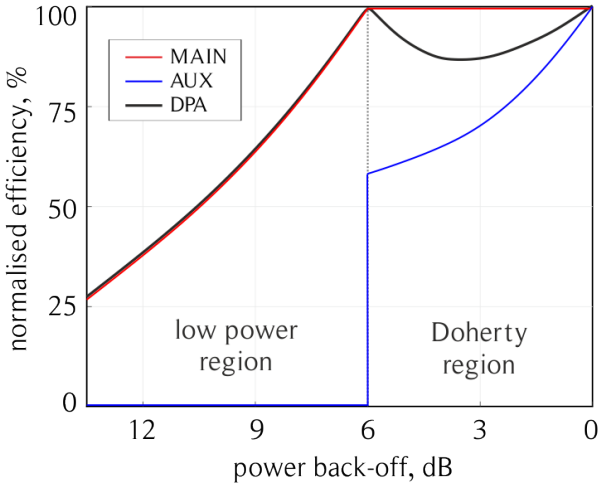


Figure 3.2: Doherty power amplifier efficiency. Curves are representative of a Class-AB/C Doherty PA.

In the original work by Doherty, the auxiliary amplifier is also assumed to be

biased in class B and turned on and off by some external circuitry. However, the implementation of such a control circuit still represents an issue, which is most often overcome by biasing the auxiliary in class C [9]. The proper selection of gate-to-source bias voltage ensures it is off at low input power and it turns on automatically at the break point. However, the class AB-C DPA is affected by some shortcomings, the most evident being that class C amplifiers provide less current than class AB ones for the same device periphery and driving level. Therefore, since equal maximum currents are required at saturation to ensure the proper load modulation, either an uneven input power splitter [59] or two different device sizes [60] must be adopted. Moreover, class C amplifiers provide lower power gain and worse linearity due to higher power-dependent gain variations.

3.2 Doherty Power Amplifier Limitations

The DPA suffers from deviations from the ideal behaviour just outlined, due to non-idealities of the active devices as well as frequency dispersion affecting all active and passive components in the architecture. Some of the main limitations that are particularly severe when it comes to modern applications are the extension of the high efficiency region, the achievable RF bandwidth and the linearity. These aspects will be briefly discussed in the following, first by reviewing some effective solutions proposed in the recent literature for the fully analog single-input topology discussed so far and then, in Section 3.3, by focusing on the dual-input topology.

3.2.1 High Efficiency Power Region Extension

The standard DPA is able to provide an efficiency peak at 6 dB OBO. However, the increasingly high PAPR of modern modulation schemes pushes towards deeper back-off levels, up to 12 dB, which are difficult to achieve with this solution.

One way to improve the High Efficiency Power Region (HEPR) is adopting an auxiliary device larger than the main one. For example, a break point at 12 dB OBO is achieved if the main amplifier reaches its maximum voltage swing at 1/16 of the maximum output power. It can be shown for the conventional two-way architecture that $P_{\mathrm{M,max}} = P_{\mathrm{DPA,max}}/\sqrt{\mathrm{OBO}}$, where OBO is expressed in linear units, i.e. as a ratio of powers. Therefore, the main amplifier delivers 1/4 of the maximum output power, while the remaining 3/4 must be provided by the auxiliary, which should therefore be at least three-times larger than the main (assuming class C bias and uneven power splitting) [27]. This solution is known as asymmetrical DPA [61, 62, 63, 64]: the higher the level of asymmetry, the wider the HEPR. However, increasing the asymmetry brings about a severe gain reduction, due to the combined detrimental effects on the overall performance of the inherently lower gain of the class C auxiliary stage and of the reduced power delivered to the main stage

because if the uneven input power splitting. Furthermore, practical limitations on the realisation of the input power splitter may come into play. For instance, if a Wilkinson configuration is considered, the unbalance between the widths of its arms increases with an increasing splitting ratio. Finally, different device peripheries call for the design of distinct input matching, stabilization and bias networks, which may easily hinder a broadband operation due to the difficulty of controlling the relative phase of the branch signals over a wide frequency range. The asymmetrical DPA solution is therefore only viable for medium HEPR, typically below 10 dB.
In [65], a combination of the asymmetrical DPA and the sequential PA solutions is proposed, achieving 10 dB HEPR. In this case, the load modulation effect is used to achieve a smoother transition from the low-power condition, where only the main is on, to the high-power condition, where only the auxiliary is on.

Alternative approaches are the multi-way and multi-stage DPA architecture [66, 67, 68, 69]. The multi-way DPA, or N-way DPA, is a variant of the asymmetrical DPA where the single auxiliary stage is replaced by $N-1$ parallel devices that turn on simultaneously, realizing an equivalent $N-1$ larger auxiliary device under the assumption that each device has a fixed periphery equal to that of the main. This solution mainly allows to overcome the issues related to the adoption of a single very large device. The efficiency, however, suffers a significant drop in the Doherty region as shown in Fig. 3.3 (a). It is interesting to compare the efficiency curves of a Doherty and a Chireix architecture designed for the same back-off level, as reported in Fig. 3.4. Case (b) corresponds to the standard 6 dB HEPR, while (a) and (c) show 3 dB and 9 dB HEPR architectures. It can be seen that both Doherty and Chireix are affected by an increasing efficiency drop as the HEPR widens. In all cases, the DPA shows sharper peaks and a more marked valley, whereas the Chireix offers a wider and shallower HEPR. On the contrary, in the low power region the Chireix efficiency decrease much more abrupt than that of the DPA. However, as discussed in Chapter 2, practical Chireix PAs are hardly operated in pure outphasing mode at very deep back-off levels, which makes this aspect relatively less critical.
The multi-stage DPA, or N-stage DPA, replicates the Doherty concept in a modular cascade configuration: the $N-1$ auxiliary stages are not connected in parallel are working simultaneously, but they turn on at different points, following a precise sequential scheme, in order to provide N efficiency peaks and $N-1$ Doherty regions as shown in Fig. 3.3. The main drawback of both these solution is the increased circuit complexity, requiring N-way splitting circuits and complex output power combining networks, especially in the case of the N-stage DPA.

Several attempts at widening the HEPR while keeping the increase of complexity to a minimum have been made, maintaining a two-stage symmetrical DPA structure. The adoption of an asymmetrical drain supply voltage [70, 71, 72, 73] is

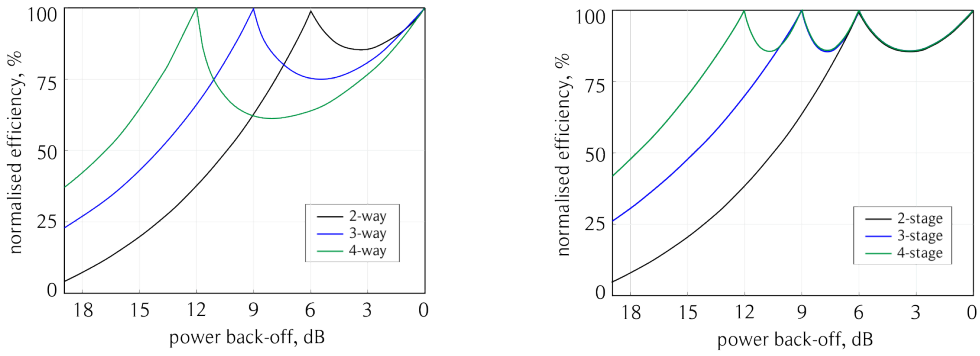


Figure 3.3: Comparison of theoretical efficiency curves of the N-way (a) and N-stage (b) Doherty amplifiers.

a viable approach. The main drawback is that the main device, whose drain voltage is lower, is under-utilized. In [74] and [75], instead, a wide HEPR is achieved by modifying the output power combiner, thus ensuring a high power utilization for both transistors, while electronically tunable devices are adopted in [76] to dynamically adjust circuit parameters as a function of the average input power level, thus maintaining high efficiency even in deep OBO. A novel technique based on adopting an output impedance for the auxiliary stage different from an open circuit and changing the phase delay of the IIN, has been recently proposed in [77].

All the HEPR enhancement solutions proposed so far have proved effective for PAPRs below 10 dB. This is often sufficient for the requirements set by modern communication standards if used in conjunction with some digital Crest Factor Reduction (CFR) algorithm that either clips or cancels the peaks of the modulated waveform to limit its PAPR [11, 12, 13].

3.2.2 Linearity and Efficiency

As already hinted at, the peak efficiency of a DPA ideally coincides with the maximum efficiency achievable by its branch PAs. It follows that the DPA efficiency can be further improved by enhancing the efficiency of the main and auxiliary amplifiers, for instance adopting some harmonic tuning approach such as second harmonic control [64] or class F harmonic terminations [78] for the main amplifier. More recently, a high-efficiency switched-mode class E/F amplifier is employed in [79] to implement both the main and the auxiliary. In [80, 81], two extremely compact output combining networks integrating harmonic load terminations are proposed, based on a lumped element and a harmonic trap network, respectively. Additionally, the possibility to exploit the odd harmonics generated in the auxiliary amplifier to shape the drain voltage waveform of the main device allowing it to

operate at a reduced supply voltage, thereby increasing efficiency, is demonstrated in [82].

Moreover, the theory of operation is based on the simplified assumption that the active devices behave as controlled current sources. In addition, the different bias conditions of the main and auxiliary devices result in different output current profiles and consequent gain imbalance and phase offset between the two stages. As a consequence of all these factors, a deviation from the optimum load modulation arises, which leads to a back-off efficiency drop and poor linearity. Most of these factors are determined by device technology and can hardly be overcome at the PA design level. However, a design strategy has been presented to mitigate the knee voltage limitation [83], which is especially severe in GaN technology.

The impossibility of having an abrupt turn-on of the auxiliary PA poses a challenge in the choice of the optimum bias conditions. Adopting an early turn-on mitigates the gain imbalance between the two stages and the distortion of the output current waveform, thus improving DPA linearity. As a positive side effect it may also extend the HEPR but, on the other hand, it sensibly lowers the efficiency peak. As a consequence, a careful trade-off between linearity and back-off efficiency is called for.

Reactive device parasitics have a major impact on the DPA load modulation, which should be transferred from the common node plane to the intrinsic drain plane to maintain a correct operation, i.e. any real impedance variation at the common node reference plane should be transformed into a corresponding real impedance variation at the intrinsic drain plane of the two devices. The ideal Doherty operation only assumes real impedances are presented at the common node, and therefore the quarter-wavelength line classically adopted as IIN can correctly transfer load modulation to the intrinsic device plane. However, the output parasitic reactances of a real device make the load seen at the device drain plane complex. If not compensated for, they prevent a correct load modulation transfer to the intrinsic drain plane. The OMN is designed to compensate the device parasitics over the desired frequency range. However, if it is designed only for one specific load impedance value, typically the value at saturation, the parasitics are not completely compensated for all other impedance values explored during the load modulation. The impedance presented at the intrinsic drain plane is therefore affected by an unwanted phase rotation [84], resulting in lower back-off efficiency and worse linearity. Moreover, in the low power condition, when the auxiliary is off, the open circuit at its drain plane must be correctly restored at the common load plane to avoid current leakage from the main device.

A widely adopted solution to restore the optimal load modulation is the offset lines technique, introduced in 2001 in [85] and depicted in Figure 3.5. It is demonstrated in [84, 86] that the insertion of two transmission lines, with characteristic impedance equal to the load impedance at saturation and of proper length, at the

output of the auxiliary and main branches forces the open circuit condition at low power levels and restores the load modulation within the whole Doherty region, respectively. The theory of offset lines is exact at a unique design frequency: the compensation effects just listed become partial when moving away from it, thus making this method not suited for very wideband operation, at least in its most basic implementation.

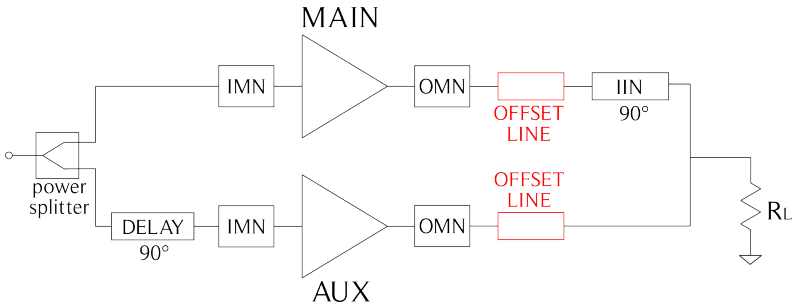


Figure 3.5: DPA schematic including matching networks and offset lines.

An alternative method to compensate for parasitic effects, which is often preferred to offset lines, especially when wideband operation is targeted, is the co-design of the OMNs and the output combiner, where the correct load modulation is imposed as an additional constraint for circuit optimization [87, 88, 89]. This approach has the additional advantage of reducing the circuit size. On the other hand, the offset lines technique is applicable to already existent PAs, which can therefore be inserted in a Doherty configuration without the need of modifying their matching networks. Both techniques are ultimately compatible with wideband applications. For instance, bandwidth enhancement is obtained by means of dual-band offset lines in [90] and with a wideband output compensator in [64]. More recently, the co-design technique has been further generalised with the adoption of a black-box approach for the entire output combiner, thus eliminating the limitation imposed by the presence of a specific IIN topology. In this way, the phase difference between the two branches becomes an additional degree of freedom which can be optimised for improved efficiency and linearity [91], enhanced HEPR [74], or wider bandwidth [92]. In the last work, the authors present the formal analysis of this novel approach and present a technique for the design of wideband power combiners that can be applied both to Doherty and to Chireix PAs.

The non-linear embedding technique is an alternative approach to account for the device parasitics during PA design. First introduced in [93, 94], it has been recently applied to the design of an asymmetric DPA [71]. The harmonic terminations for the optimum DPA performance are determined at the intrinsic drain plane (or, equivalently, at low frequency where device parasitics are negligible), thus allowing to implement waveform engineering directly. The non-linear embedding technique is then used to derive the appropriate harmonic terminations to be presented at

the extrinsic output plane (after parasitics) corresponding to the desired operation. Finally, the matching networks able to provide the required loads are synthesised.

Another non-ideal effect, which is not accounted for by the simple current-source model and which may deeply affect the DPA operation, is the power-dependence of the transconductance and the intrinsic capacitances (in particular the equivalent input capacitance). This results in a variable phase misalignment of the output currents across the Doherty region, leading to a perturbation of the load modulation and consequent power loss and phase distortion (Amplitude Modulation–Phase Modulation (AM-PM)), thus affecting both DPA efficiency and linearity. Moreover, the capacitance variations are larger for class C than class AB devices, further enhancing this undesirable effect.

Several expedients have been devised so far to mitigate this effect, such as the addition of specifically designed offset lines to enhance back-off efficiency [95], or of an offset line on the auxiliary input that especially improves linearity [96]. In [97], it is demonstrated that an extended-resonance input power divider can be effectively employed to implement an adaptive input-dependent power division between the main and auxiliary stages that compensates the phase misalignment, thus enhancing both linearity and efficiency.

Even if the above mentioned approaches have succeeded in partially enhancing the linearity of DPAs, this is still incompatible with the requirements of the current telecommunications standards. In particular, a major issue is the unavoidable AM/PM distortion due to the load modulation [98, 99, 100]. The adoption of Digital Pre-Distortion (DPD), or other linearisation techniques, is therefore mandatory in many applications [101, 102, 103, 104, 105]. The additional power consumption and circuit complexity required for linearisation raise an open question about the actual cost effectiveness of the combined DPD + DPA transmitter: while its superiority with respect to conventional transmitters has been proven in base-station applications, its applicability to point-to-point backhaul radio networks is still debated [106, 59]. Similar concerns hinder its adoption in the large antenna arrays foreseen in 5G base stations, where the output power of each PA is limited and, similarly to the backhaul case, the non-linearity of the DPA might be too strong to be handled by simple pre-distorters.

3.2.3 Bandwidth

At present, a major challenge in DPA design is to extend its bandwidth beyond one octave. Of course, the bandwidth of a PA can be determined by different FOMs. In conventional PAs, either the output power or the power gain is adopted to define the bandwidth. However, for back-off efficiency enhancement techniques such as the Doherty, a useful definition of bandwidth is the frequency range in

which the back-off efficiency peak remains within a given threshold, such as a given fraction of the maximum value achieved at centre frequency.
There are several factors impacting on the attainable bandwidth. An evident one is the dispersive nature of the employed passive networks, such as the quarter-wavelength IIN, the offset lines (where used), as well as the input and output matching networks. However, the limits imposed by these networks are seldom reached, since the strictest limiting factor to the overall bandwidth is actually posed by the output parasitic capacitances of the active devices. In fact, as one moves away from the design frequency, the impedance seen at the intrinsic drain planes deviates from the optimum value and load modulation in the Doherty region is sensibly worsened [107, 108].
An effective method to mitigate the effect of the drain capacitances is to embed them within the combining network [109]. This approach enables a significant bandwidth enhancement while reducing the circuit size [64, 89, 72].

Other methods that allow to widen the bandwidth of DPAs are the employment of non-conventional output combiners [110, 111, 112], the application of the real frequency technique [113] to the design of the output matching networks [108], and the modification of the characteristic impedance of the IIN [114, 72]. The last method aims at reducing the mismatch occurring when the load seen by the IIN is different from its characteristic impedance. In the traditional configuration, impedance mismatch occurs (at the Z_{M} plane of Fig. 3.1) at the break point, where the output impedance is $R_{\mathrm{opt}}/2$, because the IIN characteristic impedance equals the optimum load at saturation R_{opt}. It is demonstrated in [114, 72] that a wider bandwidth can be achieved by imposing that the impedance matching condition be satisfied in at the break point while moving the frequency-dependent mismatched condition is toward saturation, where the compressive behaviour of the saturated PAs ensures smaller sensitivity. A similar approach is used in [115] for a DPA that includes offset lines. In this case, the characteristic impedances of both the IIN and of the main offset lines is set equal to the output impedance at the break point, whereas that of the auxiliary offset line is kept equal to the output load at saturation, also achieving bandwidth enhancement.

Finally, in case the limited bandwidth of the IIN itself represents an issue, it is possible to replace the quarter-wavelength line with inherently wider-bandwidth networks, such as the Klopfenstein taper proposed in [114].

3.2.4 Operating Frequency

The limitations discussed above tend to become more severe as the operating frequency increases, due to the gain degradation of the active devices as well as higher losses of the passive structures [116]. Presently, watt-level DPAs based on the widespread 0.25 μm gate-length GaAs [117] or GaN [118, 89] technologies are limited to Ku-band (below 18 GHz). Few examples working in K-band (18–27 GHz) also

exist, resorting to the more performing 0.15 μm GaAs [119] or GaN [120] technologies. Above K-band, power levels around 0.5 W are attained resorting to 0.15 μm GaAs pHEMTs [121, 122].
These figures indicate that technological advancements in compound semiconductor processes are crucial to allow for the application of the DPA architecture to next-generation communication systems.

3.3 Dual input architectures

Recent developments of Digital Signal Processing (DSP) and Digital-to-Analog Conversion (DAC) techniques make mixed-signal solutions increasingly attractive, despite they were deemed unfeasible in the recent past. In this framework the dual-input DPA is emerging as a promising solution able to overcome the typical issues of the analogue DPA [123].

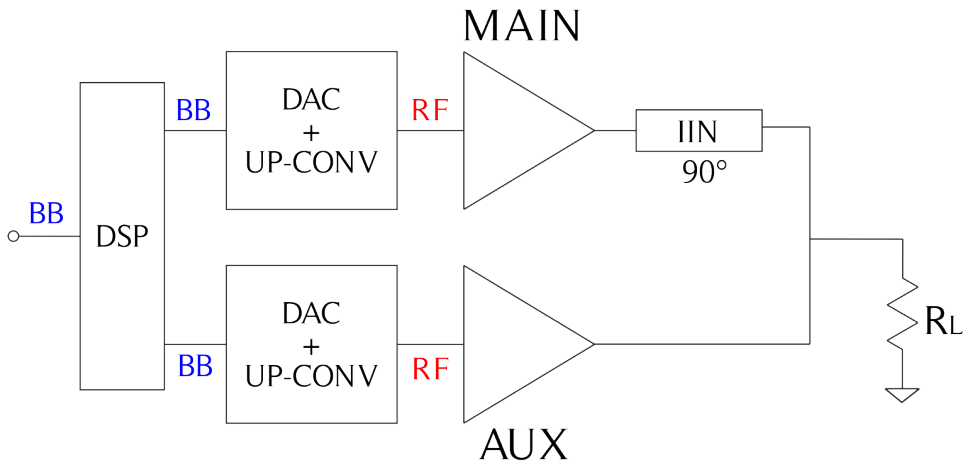


Figure 3.6: Digital/dual-input DPA scheme.

In a dual-input DPA, two distinct RF inputs for the main and auxiliary amplifiers are separately generated and controlled, as shown in Figure 3.6. The signal conversion block is duplicated, which implies higher cost and complexity, but the input analog splitter is eliminated. This enables to adapt the signal splitting and phase alignment between main and auxiliary in several ways, as a function of frequency and power, to enhance a particular aspect of the DPA performance, or to achieve a specific trade-off among several different FOMs. Concurrent optimization of different features (among efficiency, gain, linearity, bandwidth) has not been demonstrated yet. However, it is possible to reconfigure the splitting scheme according to the current system requirements.

The enhancement of back-off efficiency through adaptive power distribution and phase alignment algorithms is demonstrated in [124, 86], where minimum wasted

power when the auxiliary device is off, as well as phase-aligned output currents during load modulation, are achieved. In [125], the HEPR is improved by dynamically adjusting the amplitude and phase of the input signals, and three-input versions also exist [126] for further HEPR enhancement.
Darraji *et al.* claim that an even signal distribution in the low power region and an uneven one in favour of the auxiliary in the Doherty region, optimises linearity and flat-gain response [127]. Furthermore, a frequency dependent signal decomposition scheme is proposed in [128] to improve DPA bandwidth. A further bandwidth enhancement is obtained in [129], by resorting to a digital equalizer.
Recently, a wideband dual-input Doherty relying on a quasi- MMIC technology was demonstrated [130]. In this work, the IIN is realized as a high-pass filter to minimise the components count and the inductor losses.
Finally, Andersson *et al.* propose a mixed DPA-outphasing dual-input architecture achieving a fractional bandwidth wider than 100% [131].

Beyond the additional cost, power consumption and circuit complexity of the DSP, a limitation of the digitally-controlled dual-input DPA is the need for precise phase alignment and isolation between the two input signals. On the other hand, reconfigurability is an attractive feature of software-based systems. Additionally, the previously mentioned need for Digital Predistortion (DPD) to make DPAs compatible with the linearity requirements of the communication standards may favour the adoption of dual-input DPAs. In fact, the presence of the DSP to drive the inputs in a completely -in principle- arbitrary way would enable to perform linearisation without additional cost.

However, whether it is convenient to adopt dual RF input PAs in place of conventional single-input ones is still an open question. The following analysis is based on the systematic performance comparison of two DPAs, a single-input and the corresponding dual-input version. It aims at providing a means of estimating the performance enhancement offered by the dual-input compared to the single-input architecture, thus leading the choice of either one for a specific application.

3.3.1 Design

The starting DPA prototype on which this work is based is a single-input one, which was designed based on the topology shown in Fig. 3.7 to work in a 10 % fractional band around 3.5 GHz. Two identical 10 W packaged GaN transistors (CGH40010F) from Wolfspeed Inc. are used as active devices for the branch PAs. The main device is biased in class AB ($V_{DS} = 28\,V$, $I_D = 70\,mA$), while the auxiliary is biased in class C ($V_{DS} = 28\,V$, V_{GS} = -5.0 V). The OMNs are designed to match the 50 Ω system impedance to the optimum load for power of each device and also include the appropriate output offset lines [84]. The IMN is identical for both branches and it includes a stabilization parallel-RC circuit designed to ensure unconditional stability. The input delay line is added to the auxiliary path between

the IMN and the input splitter. This is an asymmetric structure based on a single section Wilkinson whose two arms are $\lambda/4$ sections with different characteristics impedance. It is designed to provide a main-to-auxiliary power splitting ratio of 1.2 on a 50 Ω reference impedance. This reversed uneven power splitting enhances gain and efficiency of the main amplifier, and therefore of the complete DPA, in the low power region while allowing for a shallower class C biasing of the auxiliary, which limits the gain reduction above the breakpoint [132].

Starting from the single-input PA architecture, the equivalent dual-input DPA is derived by removing the input splitter as well as the input delay line and allowing for separate feeding of the RF input signals. The comparison of the layouts of the two DPAs is shown in Fig. 3.8 (a), where the portion of the circuit that undergoes modification is highlighted. Due to the asymmetry in the layout of the starting PA, the input delays of the two branches are different in the resulting dual-input version, which however does not represent an issue as the signal phase difference can be digitally controlled and adjusted. The microstrip layouts are implemented on a Duroid 5880 substrate with 0.79 mm thickness and 2.2 relative dielectric constant, mounted on a metal carrier and SMA connectors are inserted at the RF inputs and outputs. The realised PAs are shown in Fig. 3.8 (b) and (c).

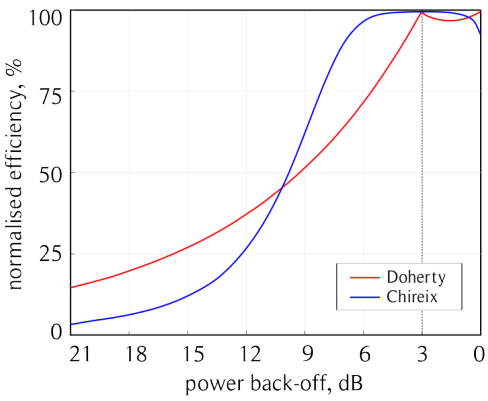
3.3.2 Small signal characterisation

Scattering parameter measurements are used as an initial assessment of the prototypes. The small signal measurements are performed using a Keysight E8361A PNA Network Analyzer. Fig. 3.9 reports the simulated and measured scattering parameters for the two DPAs, adopting the port numbering indicated in Fig. 3.8 (b) and (c). Although the two DPAs have been designed to work in a 10 % fractional band around 3.5 GHz, a 300 MHz shift between simulated and measured direct voltage gain (S_{31}) is observed in both prototypes and is therefore ascribed to some inaccuracy in the manufacturing of the output section, which is identical in the two cases. Port 1 of the dual-input DPA indicates the main branch, which is the only one that effectively contributes to the small signal gain in a class AB-C DPA. Both simulated and measured results concur in predicting a higher gain for the dual-input DPA, as expected since no power is delivered to the auxiliary branch through the input splitter. The single-input DPA, exhibits an input return loss lower than 10 dB from 3 to 3.7 GHz, with a minimum around 3.4 GHz, while some mismatch is observed in the dual-input case as a consequence of the removal of the power divider.

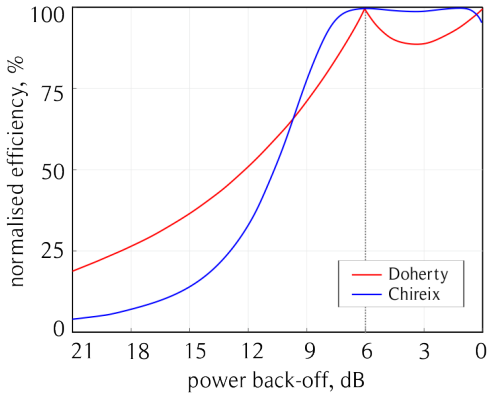
3.3.3 Optimised driving strategies

Fully flexible LUT–based driving

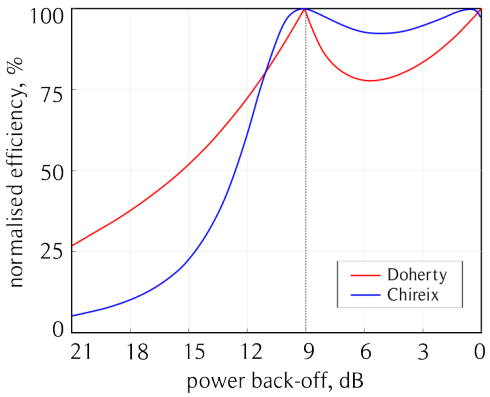
The most general and potentially beneficial driving is explored initially in simulation. The two independent inputs of the dual-input DPA are fed by signals whose power levels are $P_{\mathrm{in,m}}$ and $P_{\mathrm{in,a}} = P_{\mathrm{in,m}}/k$, where k is the splitting ratio, and whose relative phase difference is ϕ. Because its turn-on can now be controlled independently, the auxiliary device is biased on the verge of class B ($V_{\mathrm{gs}} = -3.4\,\mathrm{V}$) rather than in class C. This contributes to enhancing the gain at low power as well as easing the gain smoothing at the breakpoint, around the auxiliary PA turn-on region. At the same time, it gives a negligible efficiency penalty. An harmonic balance simulation is set up where nested sweeps of $P_{\mathrm{in,m}}$ and parameters k and ϕ are performed. The performance of the DPA at each step is recorded into a LUT, which is then to be used to determine the set of independent variables $(P_{\mathrm{in,m}}, k, \phi)$ ensuring the best performance at each power level, according to a method analogous to the one applied in [24]. This procedure is repeated at each frequency in the range 3.1–3.7 GHz, with 100 MHz steps. The focus is on two figures of merit, gain and PAE. The performance cloud corresponding to each operating condition of the dual-input PA when its input parameters are varied independently is drawn and the curves that optimise either gain or PAE are highlighted, together with the input parameters (k, ϕ) to which these conditions correspond. Fig. 3.10 shows the PAE and gain clouds of the dual-input DPA in light gray. The red curve corresponds to the highest achievable PAE (top left), the driving signals parameters that ensure such condition (right) and the corresponding gain (bottom left). Analogously, the blue curves correspond to the highest achievable gain. Finally, the dark gray curves report the behaviour of the single-input DPA. The splitting ratio k of the individual input splitter as designed on 50 Ω terminations is compared to the ratio of main-to-auxiliary power of the input signals. Their relative phase ϕ instead is evaluated, for the single-input DPA, as the phase difference of the fundamental branch currents at the input of the IMN.



(a) 3 dB



(b) 6 dB



(c) 9 dB

Figure 3.4: Comparison of Doherty and Chireix theoretical efficiency for 3 dB (a), 6 dB (b) and 9 dB (c) back-off efficiency peak.

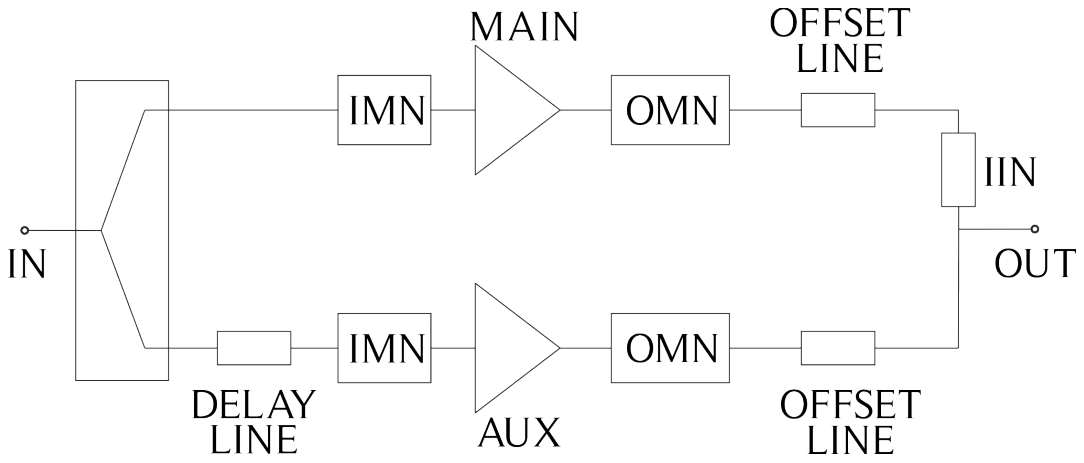
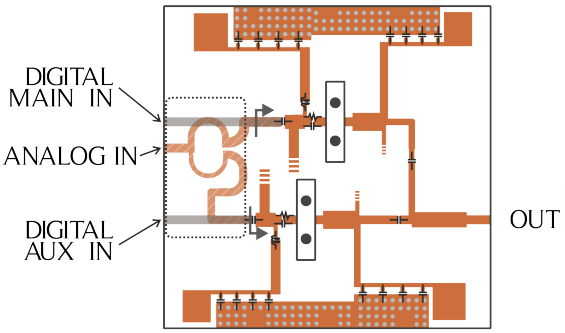
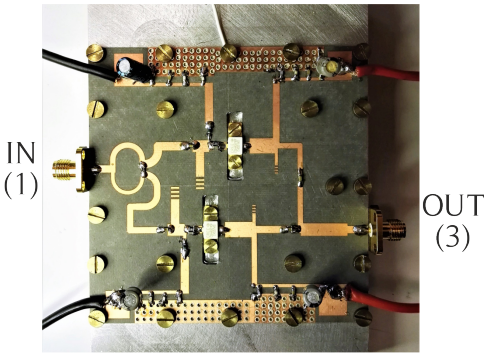


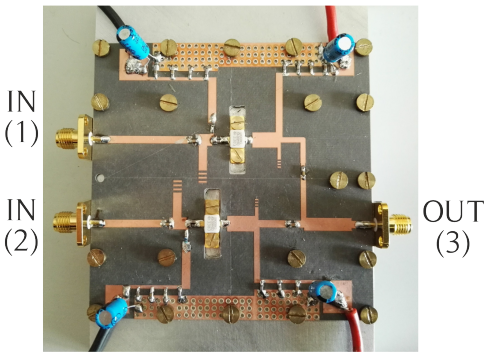
Figure 3.7: Block diagram of the original single-input DPA.



(a) layout comparison

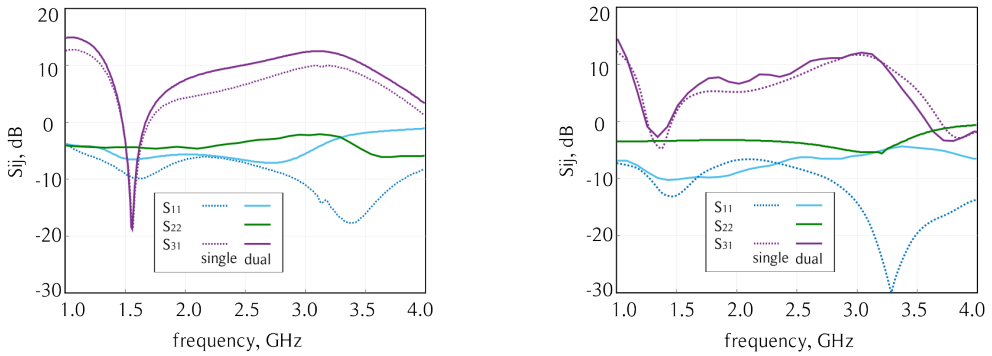


(b) single-input



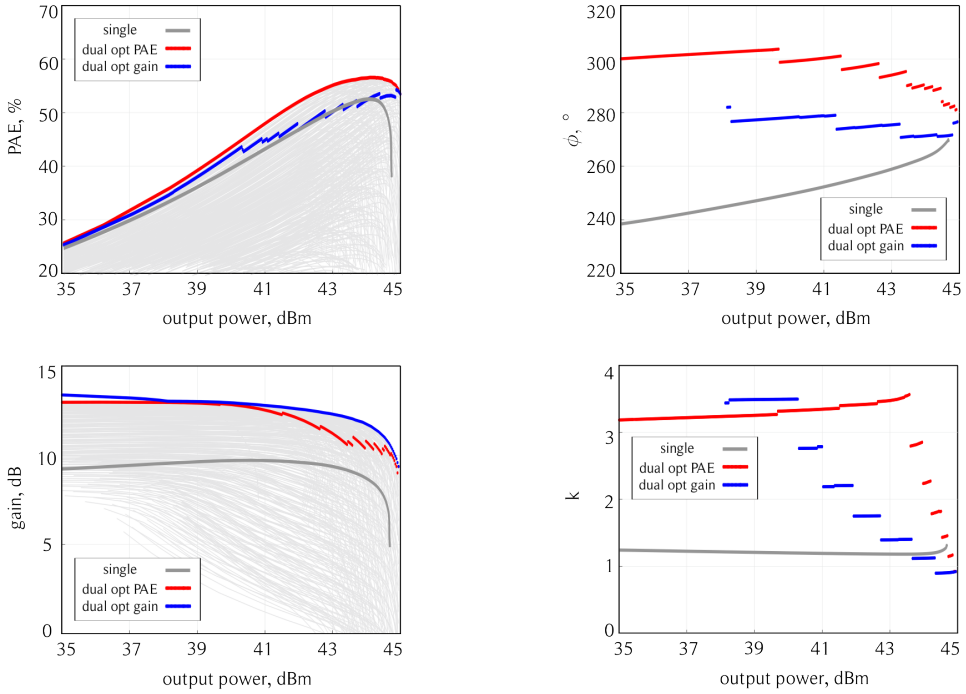
(c) dual-input

Figure 3.8: Comparison of the two analogous DPA layouts (a) and photographs of the realised single- (b) and dual-input (c) prototypes.

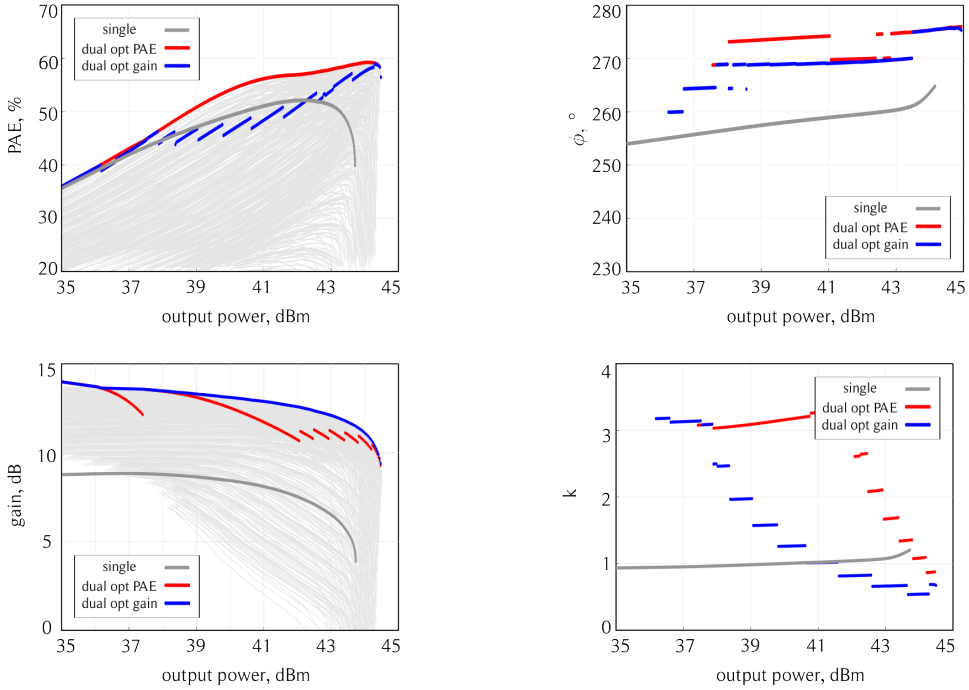


(a) (b)

Figure 3.9: Comparison of the simulated (a) and measured (b) small signal performance of the two DPAs.



(a) 3.1 GHz



(b) 3.3 GHz

An improvement of the performance in the whole Doherty region is enabled by this fully flexible driving approach, and a higher saturated output power is also achieved. In fact, dynamically controlling the phase alignment of the branch signals allows the correct combination of the main and auxiliary currents at the output summing node, thus ensuring the highest achievable power. In general, however, for a given output power level, the triplet $(P_{\mathrm{in,m}}, k, \phi)$ ensuring highest PAE does not necessarily imply the best gain performance as well. This is especially true in the high power region, after the auxiliary turn-on, whereas the red and blue curves tend to coincide at low power. This is reasonable, since the DPA operation is governed by the main at low power, and the amplitude of the signal driving the auxiliary should then be minimised, regardless of its relative phase. Focusing on the splitting ratio k, a general trend can be identified. The best efficiency is achieved, provided that the proper phase alignment is ensured, when the main PA receives more power at low output power, while the auxiliary PA is progressively fed with more and more power until it becomes dominant over the main PA in saturation. This, again, is in full agreement with the prediction based on the simplified theory presented in Section 3.1. A further information provided by this analysis concerns the turn-on speed. At all considered frequencies, a smoother and slower transition of the power splitting towards unity ensures flat gain but sub-optimal efficiency. On the contrary, the best PAE is obtained for a sharper high-to-low k transition occurring closer to saturation, resulting however in a non-negligible gain compression in the 3–6 dB OBO region. This may or may not be an issue, depending on the specific application; gain flatness is often as important a requirement as its absolute value, especially when wide channel bandwidths or multi-carrier signals are involved. As far as the relative phase ϕ is concerned, a less significant difference exists between the two optimum conditions. In most cases, the red and blue curve only differ by few tens of degrees.

Fig. 3.11 presents the performance comparison of the two PAs over the whole frequency band of interest, at saturation (a) and at 6 dB OBO (b). The fact that they are completely identical except for the input signal splitting ensures a fair comparison and allows to estimate the improvement that a dual-input architecture can bring about. Note that the curves of the single-input DPA are unique, whereas the ones corresponding to the dual-input DPA report its best performance achievable under the appropriate driving conditions, which are not necessarily the same for the different Figure Of Merit (FOM)s. As underlined above, the optimum gain and PAE conditions do not coincide in the high power region. For the sake of consistency, the saturation condition is set to be at 4 dB gain compression in both cases. For the dual-input DPA, the gain compression is evaluated with respect to the maximum small signal gain achievable at each frequency. The dual-input DPA maintains a saturated output power above 44.1 dBm over the whole targeted frequency band, against the 42.9 dBm of the single-input DPA. The saturated PAE is

Table 3.1: Comparison of single- and dual-input DPAs performance.

Freq. [GHz]		$\mathbf{P}_{\text{out,sat}}$ [dBm]	$\mathbf{PAE}_{\text{sat}}$ [%]	$\mathbf{PAE}_{\text{OBO}}$ [%]	**SS Gain** [dB]
3.1	single	44.7	43.8	35.0	10.1
	dual	44.9	54.1	38.0	13.7
3.3	single	43.4	48.9	42.8	9.6
	dual	44.1	56.7	46.22	14.7
3.5	single	43.7	42.3	43.2	8.1
	dual	44.5	58.3	51.9	14.2
3.7	single	42.9	40.5	32.7	5.9
	dual	44.3	59.3	48.6	12.6
maximum improvement		1.4 dB	18.8%	15.9%	6.7 dB

in excess of 40% and 54%, respectively. The dual-input driving offers an improvement that ranges from 7.8% at 3.3 GHz to as high as 18.8%, achieved at 3.7 GHz. Also at 6 dB OBO the digital PA has superior performance, leading to an improvement of up to 15% and maintaining it above 38% over the whole frequency band. Finally, thanks to the fully flexible DSP-based approach, the gain benefits from a significant improvement over the whole dynamic range. This is, as anticipated, mainly due to the power-dependent power splitting among the branches and the consequent possibility to bias the auxiliary device closer to the pinch-off.

Table 3.1 summarises the comparison for the frequency points reported in Fig. 3.10 and highlights the maximum absolute improvement of performance X enabled by the dual-input architecture with the respect to the conventional one, which is evaluated as $X_{\text{dual}} - X_{\text{single}}$.

Simplified driving

After estimating the degree of improvement that a fully flexible dual-input operation can offer, with the consequent increase of cost and system complexity, an attempt is made at finding simplified driving strategies that partially exploit the degrees of freedom of the dual-input architecture while maintaining some feature in common with the single-input DPA operation. On one side, this helps in simplifying the DSP and making it more robust, for instance to the unavoidable residual phase misalignment as well as unbalances and non-linear effects due to the presence of drivers, that affect the system even after calibration. Under another perspective, this simplified strategy may be used as an empirical design approach for the input network of wideband single-input DPAs, which is often affected by the inaccuracy of the non-linear model of the active devices and the consequently need of post-tuning

or re-design.

The bias adopted at all frequencies is the following: $V_{DD} = 28\,V$, $I_{D,M} = 70\,mA$ and $V_{G,A} = -3.5\,V$. It has been chosen not to exploit $V_{G,A}$ as a degree of freedom to control the auxiliary turn-on, in order to keep the setup relatively simple and as close as possible to a "conventional" DPA operation. In this way, the present characterisation campaign can be effectively exploited as a guide to re-design the input section of the DPA, with the final aim to operate it as a standard single RF input PA. Due to the frequency shift measured in small signal conditions, the large signal measurements have been performed in the frequency range 2.7–3.3 GHz. The measurement setup employed for both CW and system-level characterization is the one already introduced in Chapter 2. Its block diagram is repeated here in Fig. 3.12 for the sake of clarity. Two degrees of freedom are exploited in the characterization of the dual-input PA: a static (power-independent) phase delay and a power-dependent adjustment of the power splitting ratio between the two branches. In particular, the phase is adjusted first, using the main input signal as a reference and determining the optimum phase of the auxiliary branch at the MXG plane at each frequency in the band of interest. The corresponding phase difference at the DUT plane is calculated by calibration, i.e., by measuring a known device. In this case, a 90-degree coupler is employed and the phase settings that leads to a minimum in the transmitted power is identified, frequency by frequency. Once the optimum phase is set, the main power is swept linearly and the auxiliary turn-on point is optimized by defining a polynomial law with an arbitrary break point for the auxiliary input power, resulting in a piecewise constant splitting factor. Table 3.2 reports the optimum phase delay and splitting factor determined at the band edges and at centre frequency. The resulting optimum CW performance

Frequency (GHz)	2.7	3.0	3.3
Phase difference ϕ (°)	100	60	30
Splitting ratio k (after break point)	0.7	0.5	0.9

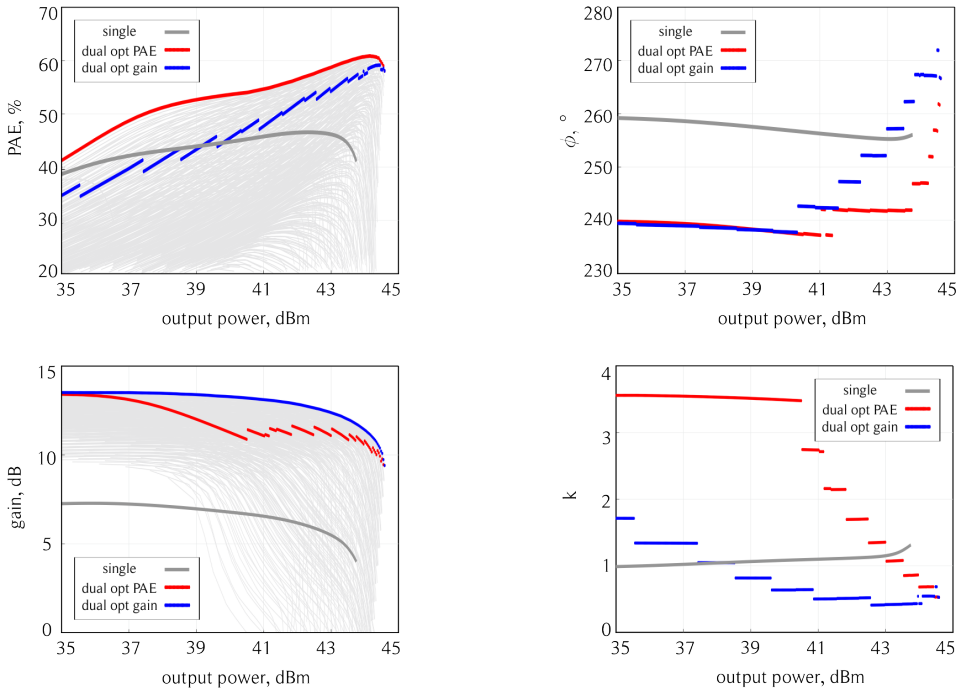
Table 3.2: Optimum input driving versus frequency for the dual-input DPA.

is reported in Fig. 3.13, where it is compared to that of the original single-input DPA. A significant improvement is visible in all cases. In particular, an increase in saturated output power of 0.2 dB, 0.8 dB and 2.7 dB is achieved at 2.7 GHz, 3.0 GHz and 3.3 GHz, respectively. This aspect is the most indicative of the effectiveness of a frequency dependent phase re-alignment in improving and equalizing the DPA performance. The possibility of feeding power to the auxiliary branch only in the proximity of its turn-on, on the other side, enhances gain and efficiency at low

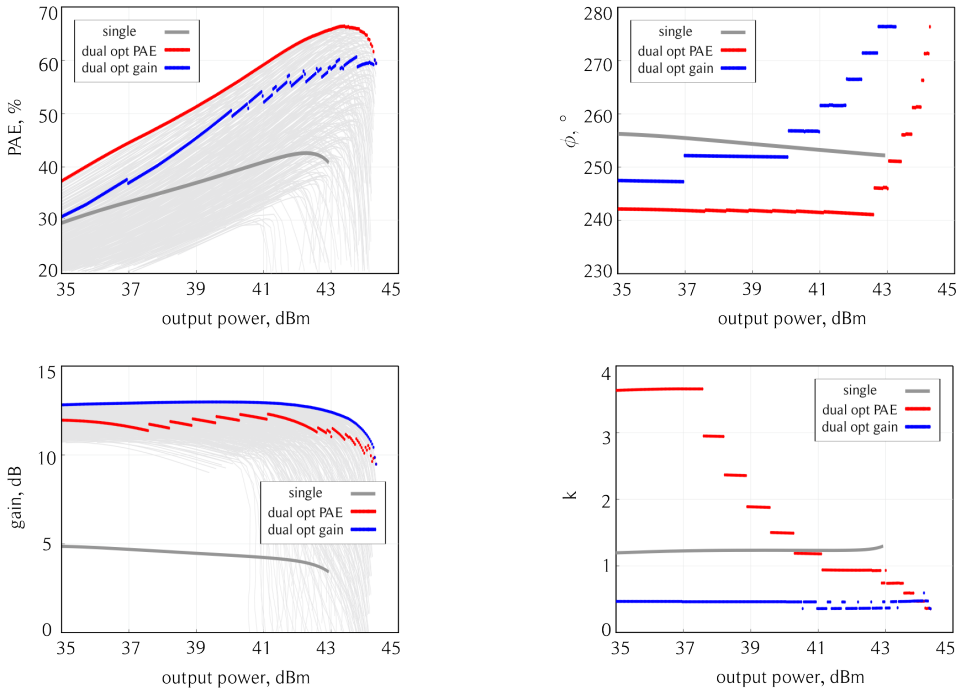
power. A gain increase as high as 2 dB is observed, while the 6 dB OBO efficiency improvement ranges from 7% at 2.7 GHz up to 30% at 3 GHz. Of course, one may only take advantage of this aspect if a digital control is maintained in the final system. On the contrary, if an improved analog input splitter is designed based on the data in Table 3.2, it is expected that the improvement in the high power region will be maintained, whereas the low power region will show slightly lesser performance due to the impossibility of completely eliminating the power fed to the auxiliary. Finally, the saturated efficiency is improved by up to 15%. It can be noted that the increment in saturated power achieved with the proposed simplified strategy is comparable to that estimated by the simulations summarised in Table 3.1. This positive outcome could be expected, since the variations of ϕ versus power at each frequency, visible in the plots of Fig. 3.10 are limited and, however, the optimum static phase in the preliminary measurement phase is determined close to saturation. Analogously the PAE improvement is similar, and in some cases even higher than, that estimated by simulations. Although an exact match is not expected, especially due to the frequency shift that makes a quantitative comparison hard to draw, this again proves the effectiveness of a simplified dual-input driving. This has the advantage of being independent of a full LUT pre-characterisation of the PA, derivable from the basic theory of operation with a reduced amount of optimisation and therefore less sensitive to small deviations or drifts in the calibration of the dual-input system. As far as the linearity is concerned, although a single tone characterisation offers limited information, it may be noted that gain flatness is worse in the dual compared to the single-input case. In fact, a compression spot that closely resembles the shape of the red gain curves in Fig. 3.10 is visible around the auxiliary turn-on region, more marked at 3 and 3.3 GHz. This is explained by the fact that the power splitting factor and auxiliary bias point have been determined in such a way as to enhance PAE at the expense of gain.

After identifying 3 GHz as the frequency point with better performance, system level characterization of the dual-input DPA has also been performed using the same setup in order to have a more effective assessment of its linearity when operated with high-PAPR modulated signals. An OFDM LTE signal with 5 MHz bandwidth and 9 dB PAPR is adopted. The optimum auxiliary phase found during the CW campaign is used, and synchronisation of the baseband streams is ensured by a pre-calibration step similar to that described for the CW measurements. A static splitting factor is applied, instead of a piecewise constant one as in the CW case, to further simplify the operation. Fig. 3.14 reports the normalized output power spectrum, before (red) and after (blue) polynomial DPD. The DPD algorithm directly acts on the main signal alone, whose predistorted version is derived after extracting the proper model. The auxiliary signal is then derived by applying the same static splitting factor that was determined in the original measurement, thus producing a “rescaled” version of the predistorted signal. Indeed, the ACPR

before DPD is limited to 21 dBc in the 5 MHz upper and lower bands adjacent to the considered channel. The linearity is greatly improved after DPD, increasing ACPRL and ACPRU to 47 dBc and 45 dBc, respectively. The average output power and efficiency are 35.9 dBm and 38%, in line with the expectation based on CW measurements.



(c) 3.5 GHz



(d) 3.7 GHz

Figure 3.10: Left: PAE and gain clouds of the dual-input DPA, with optimum PAE (red) and gain (blue) performance highlighted and compared to that of the single-input DPA (gray). Right: driving conditions corresponding to the optimum performance highlighted on the left.

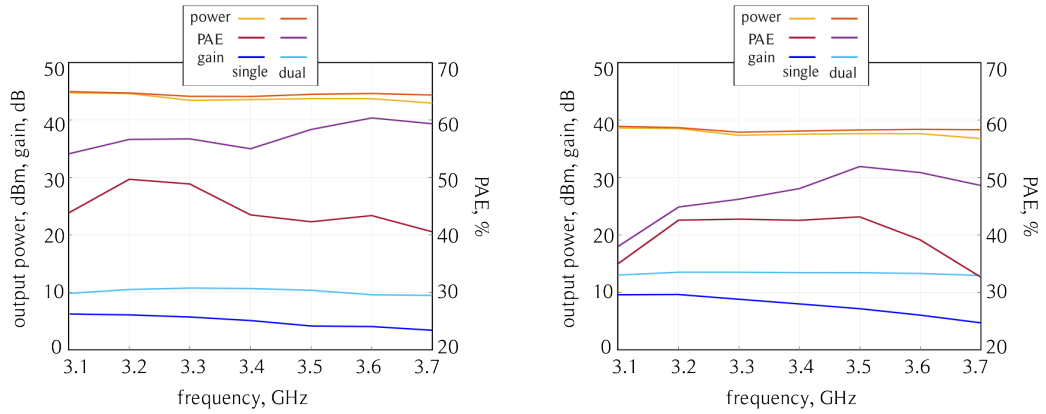


Figure 3.11: Comparison of the simulated large signal CW performance of the single- and dual-input DPAs at saturation (a) and at 6 dB OBO (b).

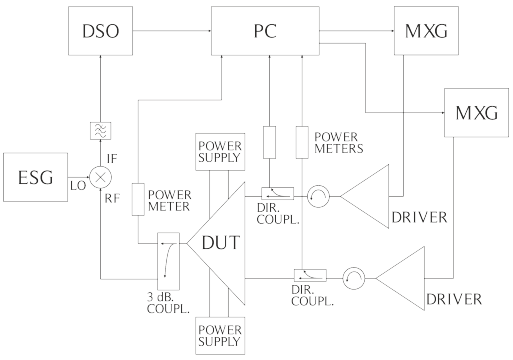
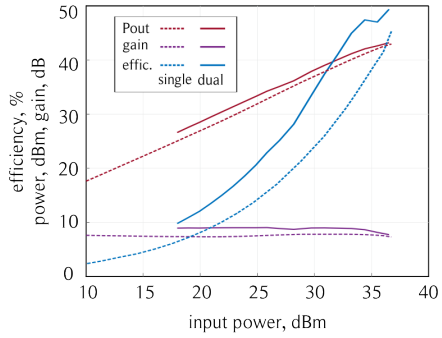
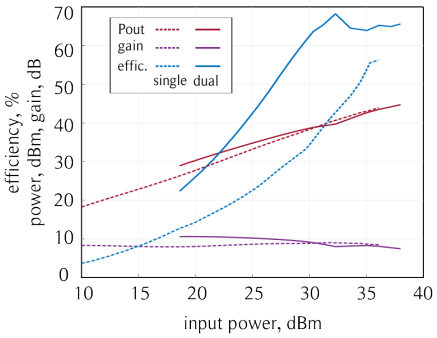


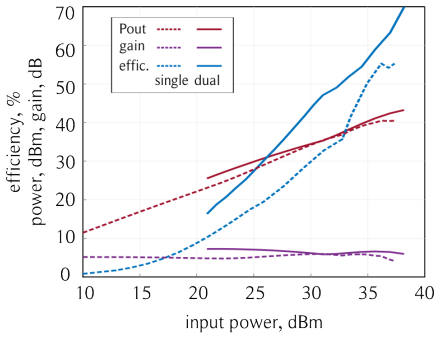
Figure 3.12: Functional scheme of the measurement setup already introduced in Chapter 2.



(a) 2.7 GHz



(b) 3.0 GHz



(c) 3.3 GHz

Figure 3.13: Measured large signal CW performance of the single (dashed) and dual (solid) input DPAs.

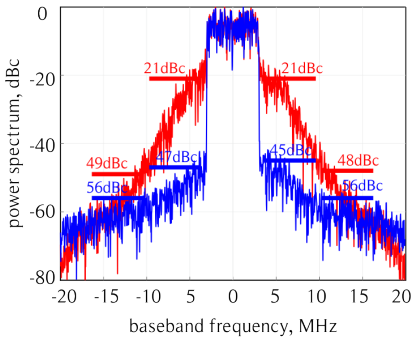


Figure 3.14: Measured output power spectrum of the dual-input DPA with 5 MHz OFDM LTE signal and 9 dB PAPR, before (red) and after (blue) DPD. Centre frequency: 3 GHz. Average output power: 35.9 dBm. Average efficiency: 38 %.

Chapter 4

The Stacked Device Topology

While Chapters 2 and 3 are devoted to the challenges posed by modern telecommunications standards from the perspectives of the circuit topology and system architecture, this Chapter approaches the subject from the technology and device standpoint. Section 4.1 is devoted to the introduction of the theoretical background necessary to the subsequent design of a stacked cell in a commercial GaAs process. The aim is to realize a multi-transistor cell whose performance in terms of breakdown (drain supply voltage) and optimum load are comparable to a single GaN transistor with analogous frequency operating range. This is presented in sections 4.2 and 4.3, which are based on the paper presented at MIKON in 2016 [133].

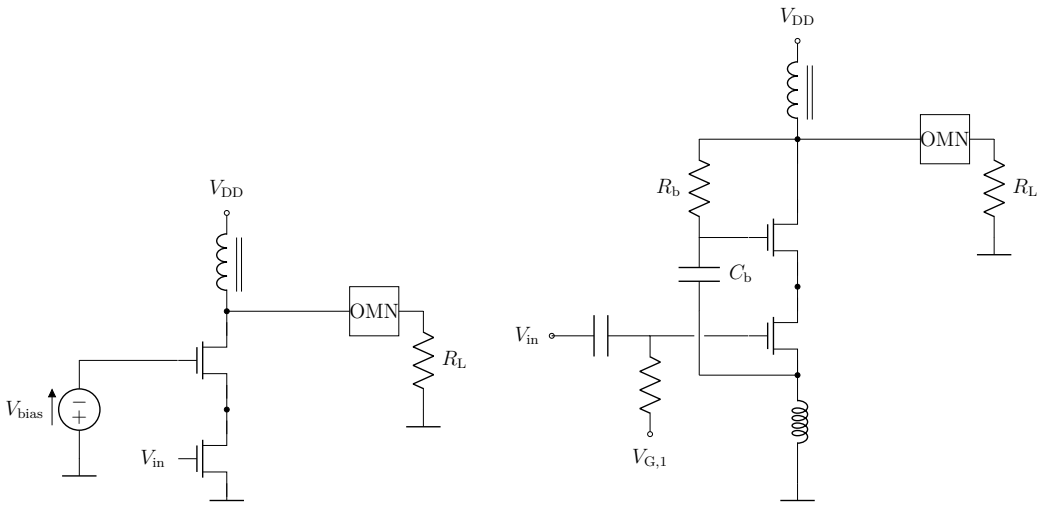
4.1 Theory

4.1.1 History

The main motivation for the employment of transistor stacks resides in the ongoing scaling of transistors, which brings about a progressive reduction of the breakdown voltage and consequent limitation of the attainable output power, for a given current level. Stacking N devices allows for an output voltage swing which is N times larger, thus achieving a N-times higher output power despite the breakdown of each cell being unchanged. An accessory advantage of this architecture is the potentially wideband operation. This is due to the low output impedance transformation ratio compared to single stage or paralleled-cells amplifiers, where the optimum impedance for power is typically much smaller than $50\,\Omega$. Before entering a detailed description of the stacked PA as currently implemented, it is instructive to review its development in the framework of power combining techniques.

Whenever a single transistor cannot provide the required output power, paralleling multiple devices and combining their power is theoretically possible. This avoids the low-breakdown issue rather than solving it, since the power level is raised by summing up all the individual current contributions while keeping the voltage

constant. The increase of the number of paralleled branches as well as the operating frequency hampers the realization of efficient power combiners, thus making this technique less viable.
The other possibility is to combine transistors in series, thus overcoming the limitation of the voltage swing dictated by breakdown mechanisms. The most widely known architecture relying on this principle is the cascode, shown in Fig. 4.1 (a). It consists of the cascade of a CS and a CG stage, whose gate is biased at an appropriate DC voltage level and it is grounded at RF. The cascode has the benefit of enhancing gain compared to the single CS stage, although in its basic implementation it suffers from limitations due to the uneven stress of the two stages. This issue has been solved by the self-biased cascode [134], which features an RF swing at the gate of the CG stage thanks the addition of a capacitor C_b and a resistor R_b, as shown in Fig. 4.1 (b). The cascode is quite popular in low frequency CMOS amplifiers as it offers a convenient way of combining two cells. However, combining three or more transistors in series requires different techniques.



(a) Cascode (b) Self-biased cascode

Figure 4.1: Schematic of the standard (a) and self-biased (b) amplifiers.

One of the earliest configurations, made up by several BJTs connected in series, was proposed by K.J. Dean in 1964 [135]. It is referred to as *bean stalk amplifier* due to the presence of a resistor ladder that biases and drives the devices. Signal propagation and consequent phase shift along the ladder makes also this technique only suited for low frequency applications.

A summary of the development of stacked transistors amplifiers from [136] is briefly recalled here. In 1985, Ezzeddine *et al.* introduced the *high-voltage Field Effect Transistor (FET) amplifier* [137], to comply with the requirements of satellite

applications and allow the complete circuit to operate under supply voltage levels higher than the breakdown voltage of each single device. This structure, shown in Fig. 4.2, is modular and can be ideally extended to an arbitrary number N of stages. It only implements stacking in DC while leaving the devices mutually decoupled at RF. As a consequence, power splitting and combining are still required at the input and output of the stack, respectively.

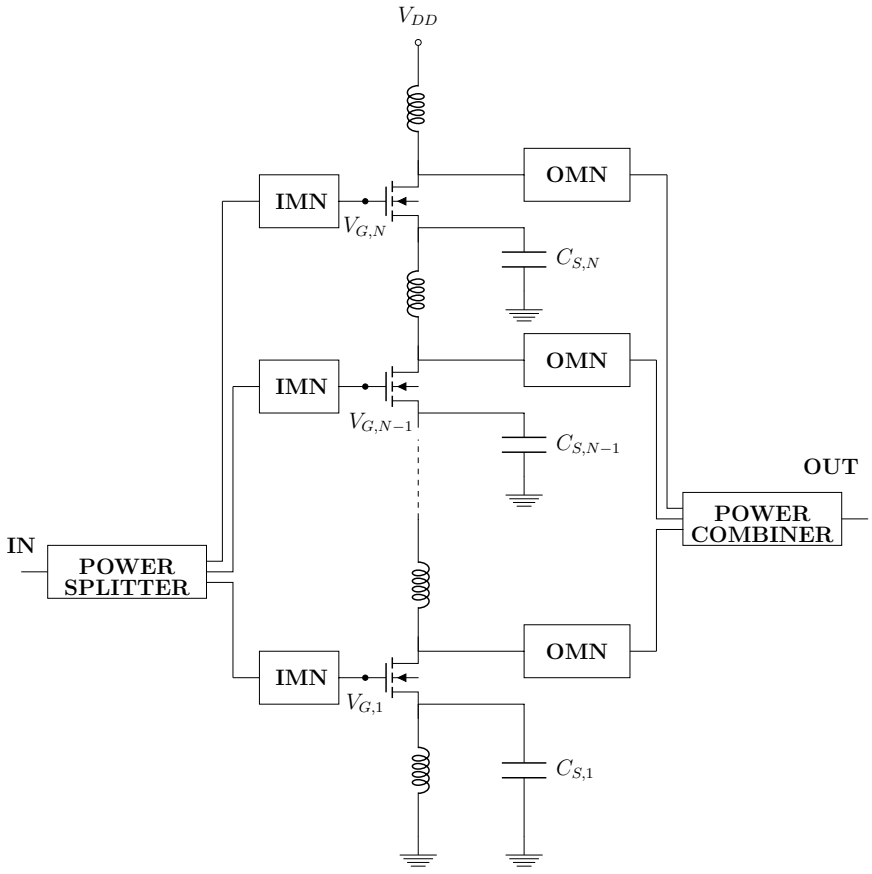


Figure 4.2: N-cell high-voltage FET amplifier.

In 1989, Peterson *et al.* [138] employed the same structure and stressed some of its issues, namely the potential instability and the risk of unbalance in the bias voltage distribution. The former is due to the large capacitive reactance presented to the FET source as a result of the gates being RF grounded and makes it essential to perform accurate stability analyses and possibly to insert appropriate stabilization networks. The latter is caused by mismatch between the characteristics of the various cells, which can be minimized by MMIC design since it ensure uniformity of the electrical characteristics of adjacent FETs. The innovative aspect of this work resides in the implementation of a four cell structure, which had never been

achieved before. In 1991, a novel bias circuitry was devised for this structure [139].

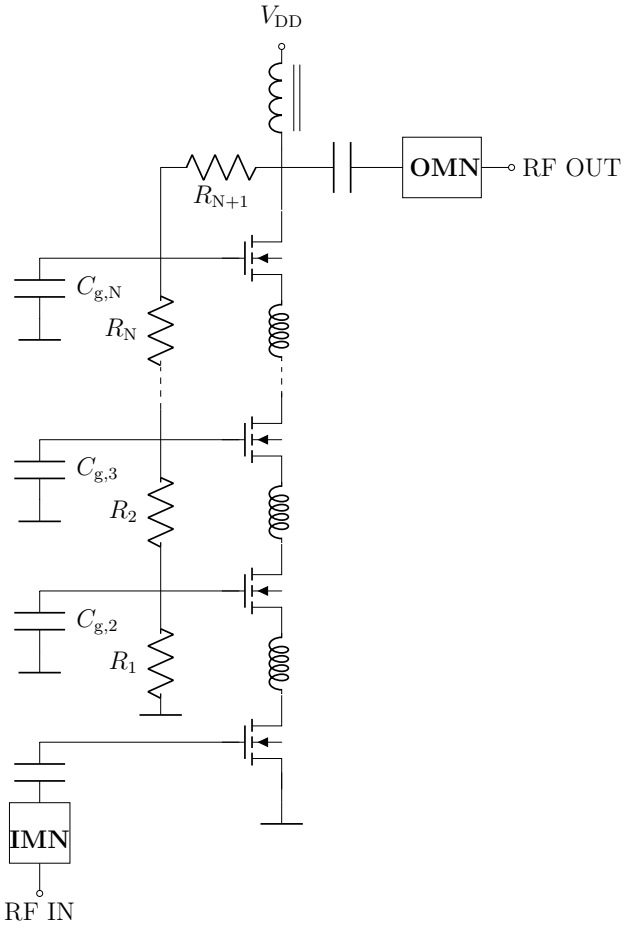


Figure 4.3: Hittite amplifier.

In 1992, Shifrin *et al.* [140] introduced the *Hittite* topology, demonstrated by a fully monolithic design at 4–5 GHz. This is the first high frequency application of DC and RF transistor stacking, with 37 dBm output power and 20% PAE achieved at 4 GHz.
Ezzeddine's high-voltage topology, which already benefited from the possibility to bias the structure at high voltage, is improved by extending the series connection to RF. The main advantages are the achievement of power combination without needing additional elements and increased input and output impedances, enabling the realisation of wideband matching networks. The configuration is reported in Fig. 4.3. A resistive ladder provides the bias to all the FETs by realizing an appropriate divider of the V_{DD} voltage, not unlike the bean stalk topology. The gate capacitors allow a RF voltage swing thus adjusting the resistance seen by the preceding cell. On the other side, the series inductors between adjacent stages

are designed to provide reactive interstage matching and therefore to align the individual voltage swings [141].

In 2003, Ezzeddine *et al.* realized the *high voltage/high power FET (HiVP)* [142], based on the Hittite topology. The authors suggest the possibility of characterizing the HiVP as a "macro-FET", with the source and gate coinciding with those of the first cell and the drain taken from the last transistor in the stack. If the voltage scale is multiplied by the number of stacked devices, the IV static characteristics of the HiVP should be coincident with the ones of the single cell.

4.1.2 Operating principle

The stacked PA architecture as analysed and implemented in this work consists of several FETs connected in series both in DC and RF. The first FET of the stack (Q_1) is a common source and it is followed by an arbitrary number of pseudo-common gate stages; the generic schematic is shown in Fig. 4.4. The term "pseudo-" refers to the fact that the gates of the Q_2, ..., Q_N FETs are not RF grounded, which is the peculiar aspect of the stacked topology as opposed to the cascode. Compared to its predecessor, the stacked has lower gain, but higher immunity to early breakdown mechanisms, as a consequence of the voltage swing allowed at each gate [143]. The overall output power is determined by the sum of the individual voltage swings of all cells, whose phase alignment must be forced by proper design. If the cells are all identical, i.e. they are made of identical FETs biased in the same operating point, each cell provides an equal drain-source voltage swing. Proper design of specific circuit elements makes the voltage swing on top of the stack to be N times larger than the swing of the individual FET. On the other side, the drain current is the same throughout the stack (exactly so in DC, while only approximately at RF due to some amount of leakage through the gate capacitors). Consequently, the overall output power is N times larger than that of the individual cell.

Bias

As the DC current is the same throughout the stack by construction, the gate bias voltages $V_{\mathrm{G,n}}$ of each cell must be such as to force the $V_{\mathrm{DS,n}}$ of all transistors to be equal. This is the case when all $V_{\mathrm{GS,n}}$ are equal. Once the bias point $(V_{\mathrm{GS_0}}, V_{\mathrm{DS_0}}, I_{\mathrm{DS_0}})$ of the elementary cell has been determined, the required DC voltage at the gate of the n-th transistor is

$$V_{\mathrm{G,n}} = \begin{cases} V_{\mathrm{GS_0}} & \text{for } n = 1 \\ V_{\mathrm{GS,n}} + V_{\mathrm{S,n}} = V_{\mathrm{GS_0}} + V_{\mathrm{D,n-1}} = V_{\mathrm{GS_0}} + (n-1)\frac{V_{\mathrm{DD}}}{N} & \text{for } n = 2, .., N \end{cases} \tag{4.1}$$

The unique drain supply voltage, to be applied at the top of the stack, is

$$V_{\mathrm{DD}} = V_{\mathrm{D,N}} = N \cdot V_{\mathrm{D,1}} = N \cdot V_{\mathrm{DS_0}} \tag{4.2}$$

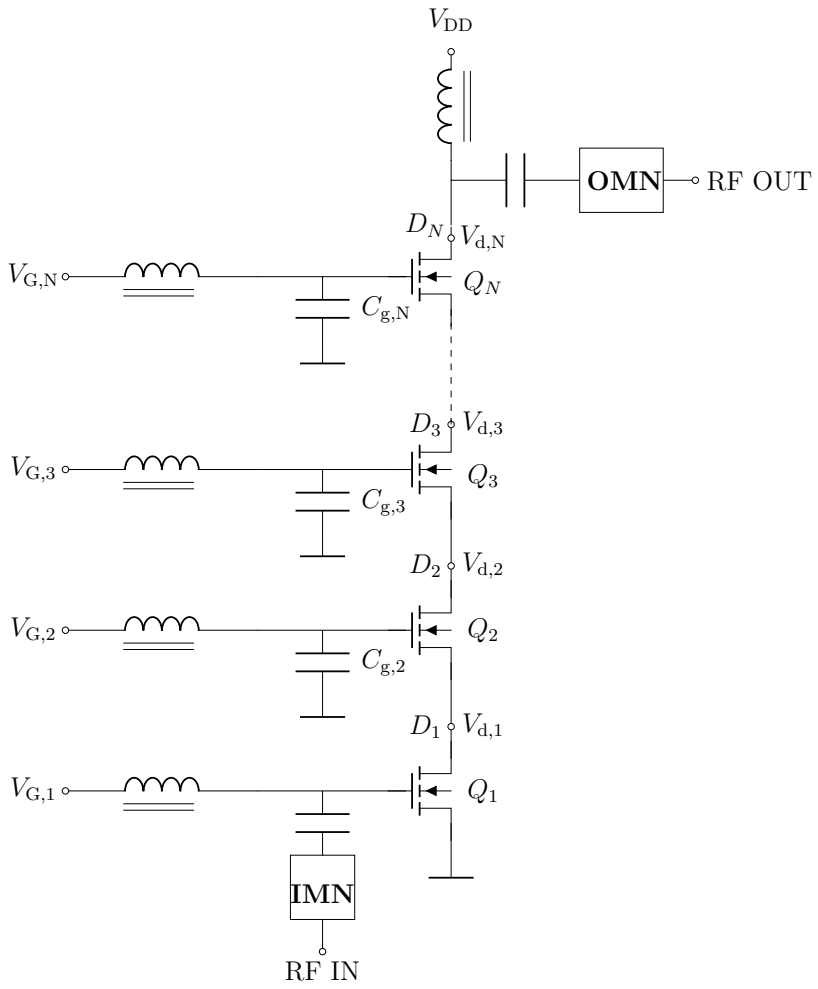


Figure 4.4: N-cell stacked PA.

where V_{DS_0} should not exceed the drain-source breakdown voltage. Breakdown issues may arise if the operating class of the individual cells is not carefully taken into account. In fact, class AB and C amplifiers have a DC current that increases with input power level P_{in}. When the gate bias chain is such as it cannot vary with P_{in}, the worst case has to be considered, which corresponds to maximum P_{in}. In this case the appropriate gate biasing is

$$V_{\mathrm{G,n}} = \begin{cases} V_{\mathrm{GS}_0} & \text{for } n = 1 \\ V_{\mathrm{GS,n}} + V_{\mathrm{S,n}} = V_{\mathrm{GS_n,sat}} + (n-1)\frac{V_{\mathrm{DD}}}{N} & \text{for } n = 2, .., N \end{cases} \tag{4.3}$$

where $V_{\mathrm{GS_n,sat}}$ is the DC gate-source voltage of the n-th cell at saturation [143]. The condition in (4.3) ensures that drain-source breakdown is not exceeded, but it does not consider gate-drain breakdown. The latter imposes an additional constraint

on the transistor size, as shown in the following derivation [143]. The gate-drain voltage of any FET in the stack can be expressed as

$$V_{\mathrm{gd,n}} = -\frac{1 + g_{\mathrm{m}} R_{\mathrm{opt}}}{g_{\mathrm{m}} R_{\mathrm{opt}}} V_{\mathrm{ds,n}}. \tag{4.4}$$

Equation (4.4) assumes that all the transistors have the same transconductance g_{m} [1] and that the n-th transistor is loaded with its optimum $\mathrm{n}\, R_{\mathrm{opt}}$. In the following, details are provided on how this condition can be imposed. It follows that, if the transistor is too small for the selected current level, the peak gate-drain voltage $V_{\mathrm{gd,n}} = |V_{\mathrm{gs,n}}| + |V_{\mathrm{ds,n}}|$ may exceed the breakdown limit.

Interstage matching

As it is made up by a number of identical cells, the stacked architecture is intrinsically modular. Once the single cell has been determined, a number of key features of the stacked PA are immediately predictable. The optimum load impedance for power is known once the bias point of the individual cell and the number of stages are known. The optimum load Z_{opt} of the individual CS stage may be determined through load pull or theoretical considerations. If the operating frequency is as low as to consider reactive parasitic effects negligible, Z_{opt} is resistive and can be derived from the slope of the static load line as $Z_{\mathrm{opt}} \equiv 1/G_{\mathrm{opt}}$, where $G_{\mathrm{opt}} = I_{\mathrm{DSS}}/\left[2(V_{\mathrm{DS}_0} - V_{\mathrm{k}})\right]$. If instead parasitic are significant, the optimum load is complex and its imaginary part is determined by the equivalent impedance of the C_{ds} at the design frequency. In this case, it is particularly convenient to reason in terms of admittances so as to decouple the considerations on load line and parasitics, because the output equivalent circuit of a transistor is made up of parallel elements. Once it has been determined, Z_{opt} fixes the ratio $V_{\mathrm{d,1}}/I_{\mathrm{d}}$. The stacking principle imposes that the n-th stage should have voltage swing equal to $V_{\mathrm{d,n}} = nV_{\mathrm{d,1}}$ and the same current I_{d} should flow throughout the stack (if the current leaking through the gate capacitor can be neglected), so that its optimum impedance is

$$Z_{\mathrm{opt,n}} = \frac{n \cdot V_{\mathrm{ds}}}{I_{\mathrm{d}}} = \frac{n \cdot V_{\mathrm{d,1}}}{I_{\mathrm{d}}} = n \cdot Z_{\mathrm{opt}}, \quad \text{for n} = 1 \ldots \mathrm{N}. \tag{4.5}$$

Standard matching techniques may be applied both at the input and at the output. Unfortunately, Z_{opt} seldom coincides with the load ensuring maximum gain. The common procedure is that of imposing the output matching first and then designing the IMN according to the maximum gain criterion.

[1] as it should be ideally for all the small signal parameters, which are fully determined by the operating point, which has to be the same for all the transistors.

In general, however, input and output matching alone do not ensure maximum output power. For this condition to be met, each FET should be provided with its own optimum impedance. The need of inserting interstage matching elements has been understood and motivated since the earliest realizations of stacked-FET PAs [140, 142].
As long as the operating frequency is low, a relatively simple approach is viable, which consists in adjusting the drain resistance of each stage by choosing the gate capacitors $C_{\mathrm{g,n}}$ properly. It has been proved by Ezzeddine *et al.* [142] that they play a key role in ensuring the optimum loading to each FET in the stack. They are designed in such a way as to form a voltage divider with the parasitic gate-source capacitance $C_{\mathrm{gs,n}}$. Analytical design formulas can be derived from the analysis of the small signal equivalent circuit of Fig. 4.5. The impedance at the source of the

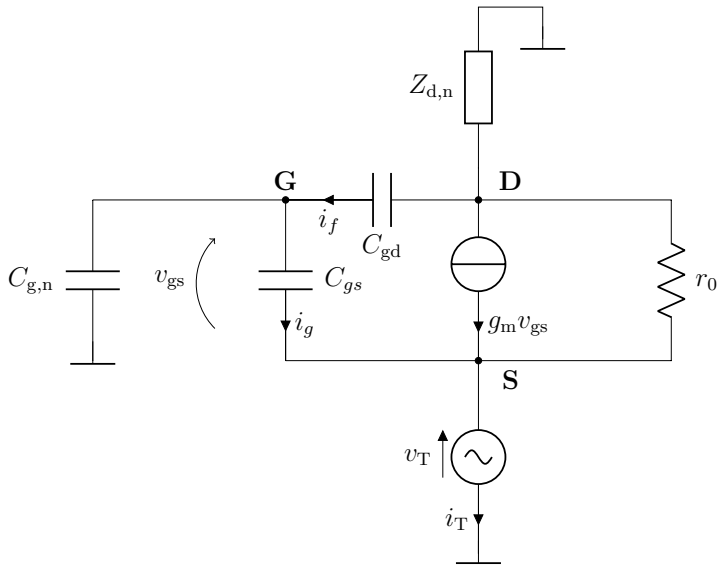


Figure 4.5: Small signal equivalent circuit for the evaluation of the input impedance of a pseudo-CG stage.

n-tn transistor is

$$Z_{\mathrm{s,n}} = \frac{C_{\mathrm{gs}} + C_{\mathrm{g,n}} + C_{\mathrm{gd}}\left(1 + g_{\mathrm{m}}Z_{\mathrm{d,n}} + sC_{\mathrm{gs}}Z_{\mathrm{d,n}} + sC_{\mathrm{g,n}}Z_{\mathrm{d,n}}\right)}{\left(g_{\mathrm{m}}sC_{\mathrm{gs}}\right)\left(C_{\mathrm{gd}} + C_{\mathrm{g,n}} + sC_{\mathrm{gd}}C_{\mathrm{g,n}}Z_{\mathrm{d,n}}\right)}. \tag{4.6}$$

If no element is inserted in the basic scheme of Fig. 4.4, $Z_{\mathrm{s,n}}$ coincides with the impedance $Z_{\mathrm{d,n-1}}$ loading the drain of the (n-1)-th cell. Some simplifications help in identifying the main dependencies. Assuming an unilateral device (C_{gd} negligible) yields

$$Z_{\mathrm{s,n}} \simeq \left(1 + \frac{C_{\mathrm{gs}}}{C_{\mathrm{g,n}}}\right) \cdot \left(\frac{1}{g_{\mathrm{m}}} \| \frac{1}{sC_{\mathrm{gs}}}\right), \tag{4.7}$$

which can be further simplified to

$$Z_{\mathrm{s,n}} \simeq \left(1 + \frac{C_{\mathrm{gs}}}{C_{\mathrm{g,n}}}\right) \frac{1}{g_{\mathrm{m}}} \tag{4.8}$$

if the operating frequency satisfies $f_0 \ll f_T$. Formulas (4.6) – (4.8) hold for $n = 2, \ldots, N$. As long as the feedback effect of C_{gd} is negligible, $Z_{\mathrm{s,n}}$ is independent of $Z_{\mathrm{d,n}}$. If so, considering that C_{gs} and g_{m} are fixed by the choice of the bias point, imposing interstage matching $Z_{\mathrm{s,n}} = (n-1)R_{\mathrm{opt}}$ allows to uniquely determine the value of $C_{\mathrm{g,n}}$:

$$C_{\mathrm{g,n}} = \frac{C_{\mathrm{gs}}}{(n-1)g_{\mathrm{m}}R_{\mathrm{opt}} - 1}. \tag{4.9}$$

Clearly, (4.9) may offer insufficient accuracy for practical applications and thus call for optimisation. This simplified analysis mainly aims at providing an understanding of which circuit elements influence the different aspects of the stack operation, so as to lead the design choices while taking advantage of CAD.

When the operating frequency is high enough for device parasitics to be significant, real matching is no longer sufficient [142, 144, 145, 146, 147, 148, 149] Reactive elements contribute to adding a phase shift to the voltage swings along the stack, so that they no longer sum in phase if no re-alignment is imposed by design. It can be proved that the optimum admittance at intermediate node between the n-th and the (n+1)-th stage, referring to the equivalent circuit in Fig. 4.5 with the addition of a parasitic capacitance $C_{\mathrm{dsub,n}}$ between the drain of the FET and the substrate, is

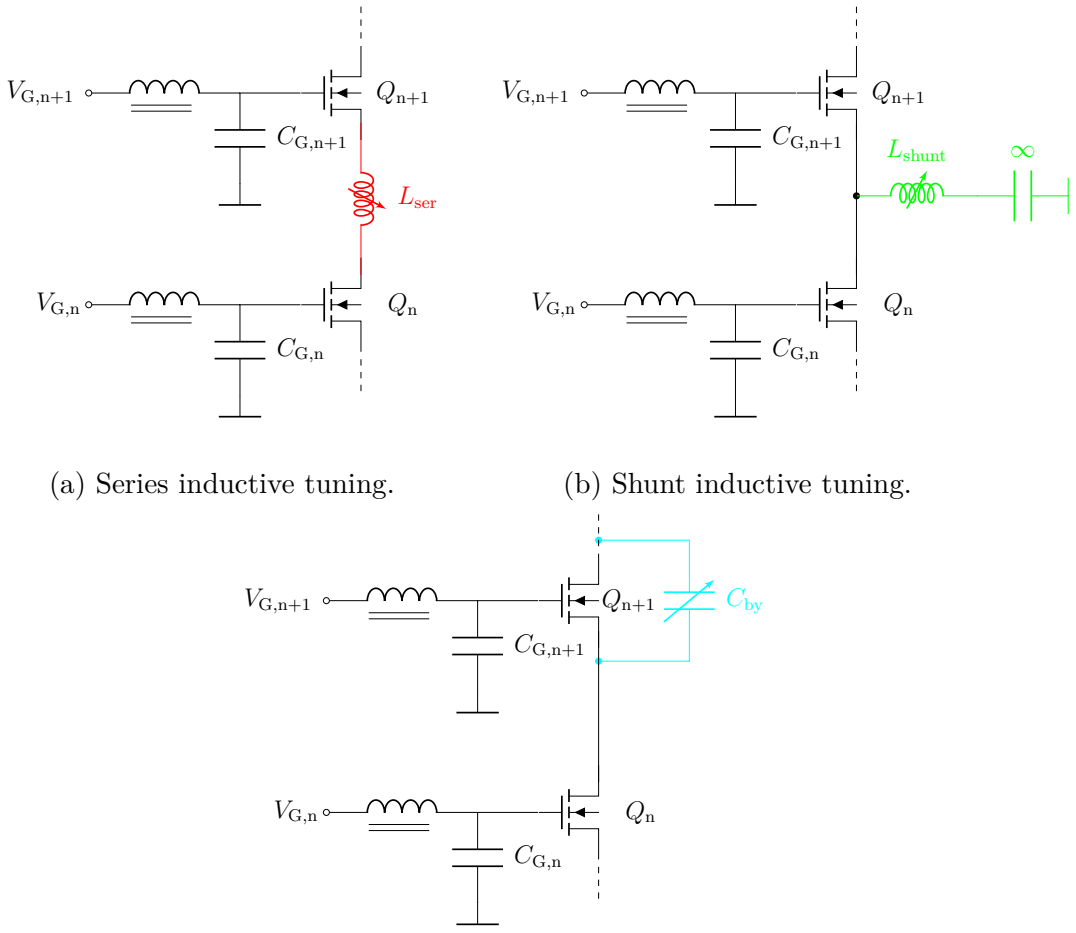
$$\begin{aligned} Y_{\mathrm{opt,n}} &\approx \frac{1}{n\,R_{\mathrm{opt}}} - \frac{j\omega}{n}\left(C_{\mathrm{ds,n}} + n\,C_{\mathrm{dsub,n}} + C_{\mathrm{gd,n}}\right) = \\ &= \frac{1}{n\,R_{\mathrm{opt}}} - \frac{j\omega}{n}\left(C_{\mathrm{eqv,n}}\right) \end{aligned} \quad . \tag{4.10}$$

Equation (4.10) suggests that the parasitic capacitances represented by $C_{\mathrm{eqv,n}}$ need to be compensated by an inductive susceptance. Note that the source of the following transistor provides a further capacitive load that contributes to worsen the misalignment [143]. Consequently, the inductive contribution has to be provided by an external element. Recent literature contains three popular reactive interstage matching techniques. The choice of either one strongly affects the design and may or may not be feasible based on several constraints, including the available technology, area occupation and compactness of the layout.

One solution consists in placing an inductor in series between two adjacent stages [150], as it is schematised in Fig. 4.6 (a). An inductor is ideally a short in DC, so the addition in such a position has the advantage of not affecting the bias point.

Another possibility is to connect an inductor between the common node between two consecutive stages and ground [149], as shown in Fig. 4.6 (b). In this case, the

inductor has to be DC decoupled by a sufficiently large capacitor for the biasing of the stack not to be dramatically modified.
Yet another solution takes advantage of the Miller effect that makes a capacitor connected between source and drain of a FET show an equivalent shunt negative capacitance at the source [148], [151]. This corresponds to the configuration in Fig. 4.6 (c).



(a) Series inductive tuning.

(b) Shunt inductive tuning.

(c) Feedback capacitive tuning.

Figure 4.6: Reactive interstage matching techniques.

Modularity

It is interesting to notice that a stacked amplifier made by N equal cells is equivalent to a single FET whose IV characteristics are analogous to those of a single FET cell, where the I-axis stays unchanged and the V-axis is scaled by N

(i.e. the drain-source voltage is N times larger) [142]. The DC characteristics of a stacked FET seen as a black-box, i.e. a "macro-FET" having as Gate and Source terminals G_1 and S_1 of the CS stage Q_1 and as Drain terminal D_N of the last pseudo-CG stage Q_N in the stack, are analogous to those of the single-FET cell it uses as a building block, with the V_{DS} axis scaled by N. In fact, the knee voltage for the stacked turns out to be $V_{\mathrm{k,cell}} = NV_{\mathrm{k,cell}}$ and the DC current is the constant throughout the stack.

4.2 Design

4.2.1 Technology

The technology selected for this work is the 0.1 μm PP10-10 Indium Gallium Arsenide (InGaAs) pHEMT process by WIN Semiconductors. It is a high-frequency process suitable for operation up to W band, featuring 4 V drain supply voltage, maximum transconductance and current density higher than 700 mS/mm and 750 mA/mm, respectively. Some relevant process parameters are listed in Table 4.1.

Table 4.1: Process parameters.

Parameter	Description	Unit	Value
$G_{\mathrm{m,max}}$	Maximum transconductance	mS/mm	755
$I_{\mathrm{D,max}}$	Maximum drain current density at $V_{\mathrm{gs}} = 0.5\,\mathrm{V}$	mA/mm	760
$I_{\mathrm{D,SS}}$	Drain current at $V_{\mathrm{gs}} = 0\,\mathrm{V}$	ma/mm	520
V_{DG}	Gate-drain breakdown voltage	V	9.6
V_{po}	Pinch-off voltage	V	-0.725
V_{to}	Threshold voltage at $I_{\mathrm{d}} = 1\,\mathrm{mA/mm}$	V	-0.95
f_{t}	Current gain cutoff frequency at $V_{\mathrm{ds}} = 1.5\,\mathrm{V}$	GHz	130

4.2.2 Topology

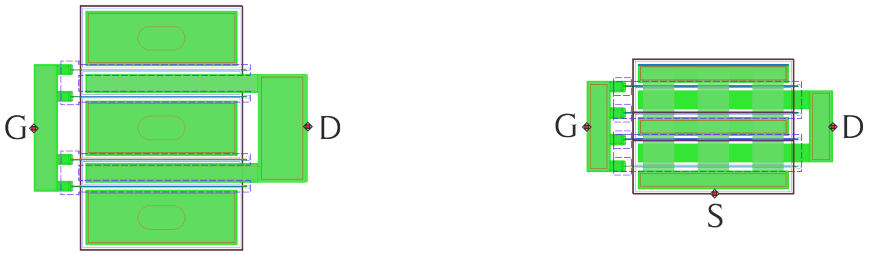
Given the 4 V maximum drain voltage, a stack of three transistor cells allows to reach an overall supply voltage of 12 V, compatible with MMIC GaN on Silicon (Si)/Silicon Carbide (SiC) processes with comparable gate length. For an initial assessment on the technology, a design frequency (10 GHz) comparatively low with respect to the cutoff frequency of the process is selected, to minimize the impact of parasitics. The aim is to provide a stacked cell to characterise through source and load pull, in order to subsequently employ it as a macro-device in the design of a power amplifier MMIC. The selected device size is $4 \times 100\mu$m, biased in class AB with $V_{\mathrm{DS}} = 4\,\mathrm{V}$ and $I_{\mathrm{D}} = 50\,\mathrm{mA}$, corresponding to 15% of the saturation current

$I_{D,SS}$. The expected saturated output power of the single device is therefore around 0.25 W, i.e. 24 dBm. According to the stacking principle illustrated in 4.1.2, the overall saturated output power should be approximately three times larger, i.e. 28.8 dBm.

The foundry provides two different configurations for the power transistors: the grounded-source (microstrip, MS) and the floating-source (coplanar, CPW) version, shown in Fig. 4.7. The difference between the two layouts is that ground vias for the MS-type device are distributed throughout the structure, thus avoiding air-bridged connections between the different source pads, which are instead present in the CPW-type device. The choice of the CPW version is the only option for the pseudo-common gate stages, which need to have all of the three terminals floating. However, it should be noted that, according to the DK manual, the CPW transistor model has been validated for common source configuration only. Therefore some inaccuracies may be expected when using it in a stacked structure, hence the need of building and characterising a test cell before carrying out the design of a complete amplifier. On the contrary, for the first stage, i.e. the common source stage, the MS version is used. Despite this causes a slight irregularity in the layout, it has been preferred to ensure more efficient ground connection and heat dissipation.

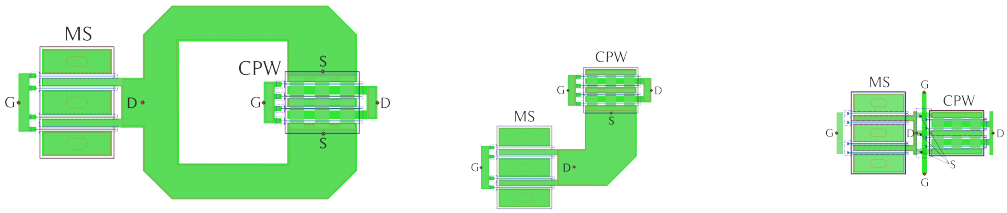
As far as the connection of the three transistors is concerned, several possible strategies are sketched in Fig. 4.8. Solution (a) does not alter the native layout of the transistors and it connects the drain of one stage to the upper and lower source ports of the consecutive one. Note that the size of the fork is exaggerated here for clarity. Indeed, the fork may be significantly shorter and, instead of allocating space for the gate capacitor inside the fork itself, it could be placed at either side by extending the gate line vertically by means of air bridges. A strategy of this kind is adopted in [80]. In the type (b) layout, a 90° bent line connects the drain (rightmost terminal) of the first stage to the source of the following stage, either from below or from above. The line length is determined by a trade-off between compactness and the need of allocating enough space for the gate capacitor and bias network. This solution also maintains the transistor cell unchanged and it trades symmetry for an increased compactness and crosstalk immunity [152]. Solution (c) has been preferred to maximise the compactness of the cell as well as to minimise the parasitic effects [153], thus leading to the modification of the standard foundry HEMT layout to provide minimum-length interconnections between drain and source of adjacent transistors. In fact, the standard layout provides source pads on the upper and lower sides while the drain pad is located on the right side of the device, hence making a short connection infeasible. The removal of the drain and gate pads on the n-th and (n+1)-th HEMTs, respectively, allows for minimum length air-bridge interconnections between the drain of the n-th stage and the source of the (n+1)-th. The gate line on a lower metal layer is extended laterally on both sides, where the bias voltage is given and room for the required gate capacitances is allocated. A detail of the air bridge interconnection of two adjacent transistors is illustrated

in Fig. 4.9. Depending on the value of the gate capacitors needed to ensure the proper operation and consequently on their size, a possibility is to duplicate each $C_{g,n}$ into two elements of half value on both sides of the gate line of the transistor. While it may not always be feasible, this option favours symmetry and stability as a consequence. A further advantage of the air bridge topology is that it is fully modular, thus allowing to potentially cascade any number of CPW devices adopting the same structure.



(a) MS (b) CPW

Figure 4.7: Available transistor configurations.



(a) fork (b) line (c) air bridge

Figure 4.8: Stacked connection strategies.

4.2.3 Stabilisation and interstage matching

In a load pull-oriented design, achieving broadband unconditional stability is fundamental to ensure that the cell be measurable under all possible loading conditions. While large signal stability can be checked after the design rather than imposed during the design phase, small signal stability can be ensured both inside and outside the operating frequency range by means of frequency selective networks. Input stabilisation is usually preferred in PA design to minimise the impact on gain and output power. A series input resistance acts at all frequencies, whereas a parallel RC block in series has an effect that is significant at low frequency and eventually vanishes at high frequency (roughly above the cutoff frequency $f_c = 1/(2\pi RC)$).

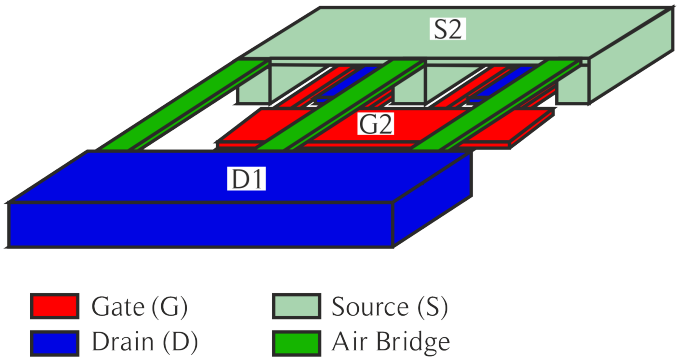


Figure 4.9: Detail of the air bridge interconnection.

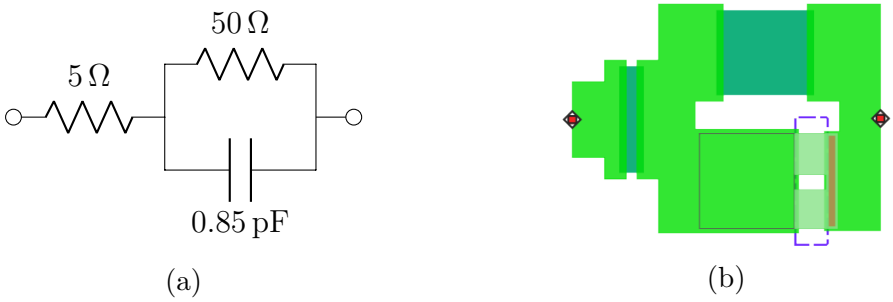


Figure 4.10: Input stabilisation network.

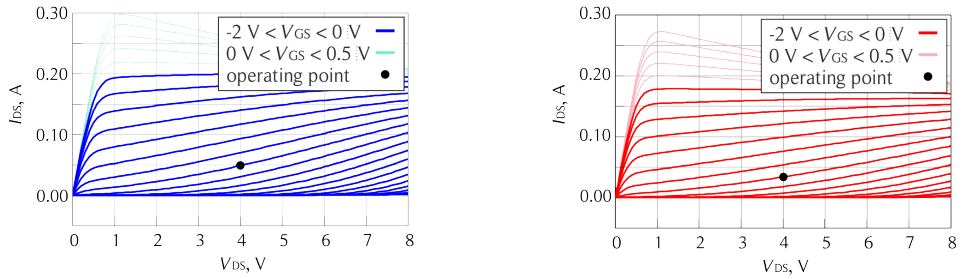
The employed stabilization R-CR network is shown in Fig. 4.10. The 5 Ω one is a TaN thin film resistor (TFR), while the 50 Ω is a mesa resistor. The capacitor is a metal-insulator-metal (MIM) structure whose nominal value is 0.85 pF. EM simulations allow to estimate its effective value at 10 GHz, which results to be around 0.94 pF, and to identify its self resonance around 32 GHz. The R-CR network is in series to the gate of the first stage, where it causes a gain reduction of less than 2 dB. While the common source cell can be stabilised by means of conventional techniques like the one just illustrated, the stability of the overall stack depends on the loading conditions of each of the (n-1)-th cells. In fact, recalling (4.10) the presence of the following pseudo-common gate stage makes the impedance seen by the preceding transistor capacitive. Therefore, the choice of the gate capacitances $C_{g,n}$ will not only affect matching - i.e. power combining efficiency - but stability as well.

Matching in a stacked PA involves enforcing the proper loading condition to each of the $N-1$ cells, as shown in the analysis of Section 4.1.2, as well as the conventional output matching at the drain of the last cell and input matching at the gate of the first cell. No OMN is designed here, because the stacked cell optimum load is to be assessed through a load-pull campaign. However, the theoretical

optimum load admittance Y_{opt} of the single HEMT must be evaluated in order to properly design the gate capacitances $C_{\mathrm{g,n}}$ of the pseudo-common-gate stages. The theoretical optimum admittance of the MS device is $Y_{\mathrm{opt,MS}} = (33 - j12)\,\mathrm{mS}$. The real part G_{opt} of Y_{opt} is obtained from the slope of the static load line, with $I_{\mathrm{DSS}} = 200\,\mathrm{mA}$ and a knee voltage of 1 V. The imaginary part B_{opt} is the one that resonates out the output (drain-source) capacitance, which is around 180 fF, at the design frequency of 10 GHz. The value of C_{ds} is estimated from the output admittance extracted in small signal when the device is biased at nominal V_{DS} and $V_{\mathrm{GS}} < V_{\mathrm{po}}$ (see Fig. 4.12). For the CPW device, instead, the simulated I_{DSS} is slightly lower, and so is the drain-source capacitance (150 fF), yielding through the same derivation to an optimum admittance of (25-j9) mS. As expected, the impact of the output capacitance increases with frequency and it is still sufficiently limited at 10 GHz, since the adopted process is conceived for operation up to W band. To maintain the structure as close as possible to the theoretical one and therefore be able to apply the closed-form design formulas presented in (4.5), the same real optimum load conductance equal to $G_{\mathrm{opt}} = 25\,\mathrm{mS}$ is assumed for all the stages. By doing so, the optimum load of the second stage in the stack is simply $G_{\mathrm{opt}}/2$. Due to this simplification, according to (4.9), only the gate capacitances are required for interstage matching with no need of other elements. A gate capacitance $C_{\mathrm{g,2}}$ on the second stage of 170 fF matches the first stage to G_{opt}, while a gate capacitance $C_{\mathrm{g,3}}$ on the third stage of 60 fF matches the second stage to $G_{\mathrm{opt}}/2$. Similarly, the theoretical optimum load of the third stage would be $G_{\mathrm{opt}}/3$, but in this case the last stage is simply terminated on 50 Ω and a more accurate value is going to be extracted through load-pull. The values of both capacitances are so low as to make the symmetric solution with $C_{\mathrm{g,n}}/2$ on each side of the drain line infeasible. The solution with a single capacitor on one side is selected, leading to the layout shown in Fig. 4.14. While $C_{\mathrm{g,2}}$ is a single $20\mu\mathrm{m} \times 20\mu\mathrm{m}$ MIM capacitor that shares the ground via with the MS transistor, $C_{\mathrm{g,3}}$ is implemented by two $17\mu\mathrm{m} \times 17\mu\mathrm{m}$ MIM capacitors in series, in order to comply with the minimum size indicated on the design kit manual and minimise the effect of process variations on the value of the capacitance.

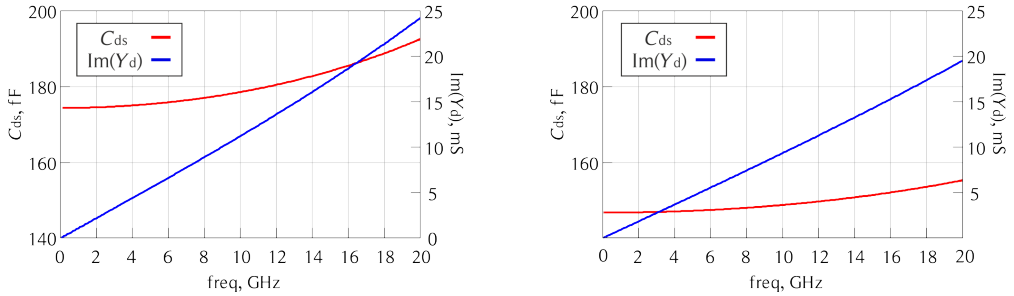
4.2.4 Bias

Given the selected bias point for the common source stage, i.e. $V_{\mathrm{DS}} = 4\,\mathrm{V}$ and $V_{\mathrm{GS}} = -0.7\,\mathrm{V}$, which corresponds to the desired $I_{\mathrm{D}} = 50\,\mathrm{mA}$, the gate bias voltages of the following stages and the unique drain supply are derived from (4.1) and (4.2), respectively. The resulting values are $V_{\mathrm{G,1}} = -0.7\,\mathrm{V}$, $V_{\mathrm{G,2}} = 3.7\,\mathrm{V}$, $V_{\mathrm{G,3}} = 7.7\,\mathrm{V}$, $V_{\mathrm{DD}} = 12\,\mathrm{V}$. Unless a self-biasing structure such as the resistor ladder in [140] is employed, which is not the case here because it has been chosen to maintain as many degrees of freedom as possible for the characterisation, each stage has to be provided its gate bias voltage. On the contrary, the drain supply voltage is only



(a) (b)

Figure 4.11: DC IV characteristics of the MS (a) and CPW (b) $4 \times 100\mu$m devices.



(a) MS (b) CPW

Figure 4.12: Output susceptance and drain-source capacitance of MS (a) and CPW (b) devices.

applied to the top of the stack, whereas the intermediate cells should automatically adjust to the proper drain quiescent voltage when their gate voltage is provided. As a consequence, the dynamic DC component of the drain voltages $V_{\mathrm{D,n}}, 1 \leq n < N$ is not fixed but rather it is free to adjust according to the change of conduction angle when input power is increased. Voltages $V_{\mathrm{G},1}$ and $V_{\mathrm{D,N}}$ are provided through the RF coplanar probes, thus resorting to external bias-tees, whereas separate DC paths for $V_{\mathrm{G},2}$ and $V_{\mathrm{G},3}$ are provided, including on-chip bias-tees. The large capacitors towards the bias pads (2.3 and 7.8 pF, respectively), which share the same ground via for compactness, are designed to provide a low impedance path to ground to the RF signal. The 2.3 pF capacitor resonates with the parasitic inductance of the ground via, whose value is around 0.1 nH, close to the operating frequency. The 2.3 nH inductor then transforms the RF short to a high impedance at the junction node with the gate capacitor $C_{\mathrm{g,n}}$, so as not to affect the interstage matching while providing a DC path for $V_{\mathrm{G,n}}$. Indeed, the inductor introduces a phase shift of 90° at 10 GHz, as illustrated by its S_{21} in Fig. 4.16 (a). These transformations are sketched in Fig. 4.16 (b). Given the low design frequency, the size of the lumped inductor on each of the bias paths is considerable. A 77 Ω resistor is also added on the DC path, between the first capacitor to ground and the DC pad, to improve

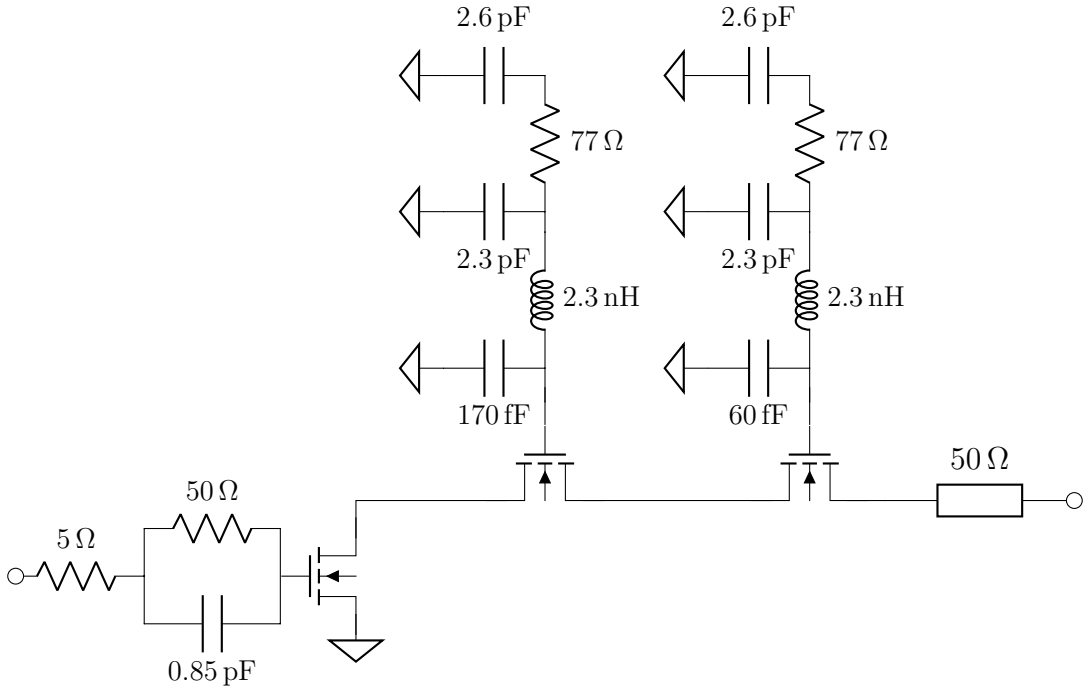


Figure 4.13: Schematic of the 3-stage stacked cell.

low frequency stability. The realised bias network makes the MMIC insensitive to any off-chip impedance variation for frequencies above 5 GHz. The decoupling at lower frequency will have to be achieved through off-chip bias tees.

The complete schematic of the realized MMIC is reported in Fig. 4.13. The MMIC layout shown in Fig. 4.14 occupies an area of $0.9 \times 0.6\,\mathrm{mm}^2$ including probe pads, whereas the dimensions of the stacked cell alone are $440\,\mu\mathrm{m} \times 155\,\mu\mathrm{m}$ (minimized width × height of the MS HEMT). The microscope photograph of the realized MMIC (mirrored with respect to the horizontal axis) is shown in Fig. 4.15.

4.3 Simulations

Single tone CW simulations have been performed to verify the behaviour under ideal biasing conditions, i.e. $V_{\mathrm{G},1} = -0.7\,\mathrm{V}$, $V_{\mathrm{G},2} = 3.7\,\mathrm{V}$, $V_{\mathrm{G},3} = 7.7\,\mathrm{V}$, $V_{\mathrm{DD}} = 12\,\mathrm{V}$.

Fig. 4.17 reports the behaviour of the stack when $Y_{\mathrm{d},3}$ equals one third of the optimum load of the CPW device. For this initial assessment, $Y_{\mathrm{d},3}$ is implemented in simulation by an ideal frequency independent element with the desired value. As shown in Fig. 4.17a, the structure is biased and loaded in such a way as to bring the three stages in the same operating conditions. In fact, they have approximately the same drain-to-source voltage swing. Consequently, the voltage swing at the

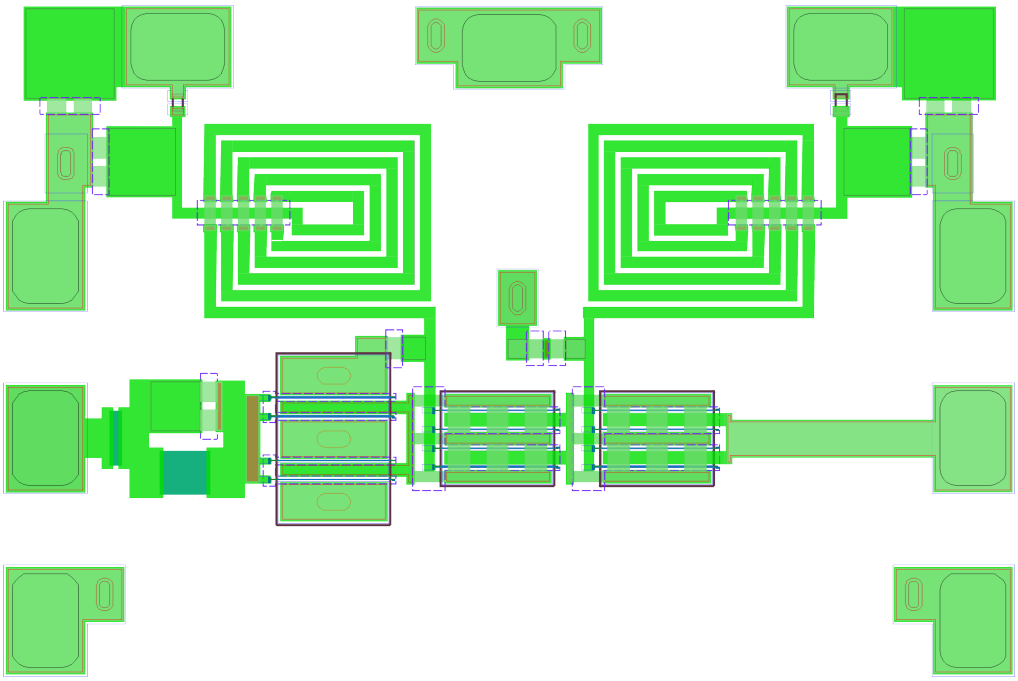


Figure 4.14: Complete layout of the 3-stage stacked cell.

drain of the second and third stage is twice and three times as the one of the CS stage, as confirmed by Fig. 4.17a. Their output power is therefore expected to approximately follow the same trend. Fig. 4.17c reports the power characteristics of each stage. It can be seen that the second stage outputs a power (24.7 dBm at 1 dB gain compression) approximately 3 dB higher than that of the first stage (21.8 dBm at 1 dB gain compression). Similarly, the third stage outputs a power (26.3 dBm at 1 dB gain compression) 1.6 dB higher than that of the second stage, which is close enough to the ideal 1.8 dB power increase if the overall output power were exactly three times larger than that of the individual stage. This small discrepancy can be ascribed to two effects. One is a slight phase misalignment between the waveforms, leading to a suboptimal signal combination. The other is the unavoidable current leakage through the gates, which are not RF grounded, thus making the RF drain current not exactly equal throughout the stack. The corresponding power gains are shown in Fig. 4.17d.

After verifying the expected operation, the optimum loads are identified through a load-pull simulation. The load is synthesised by a variable element at fundamental, while all the higher harmonics are shorted. The input power is swept and the points at same level of gain compression is then identified. Fig. 4.18 reports the contour plots for the explored subset of loads around the theoretical optimum previously identified. In fact, the load yielding highest saturated power turns out to

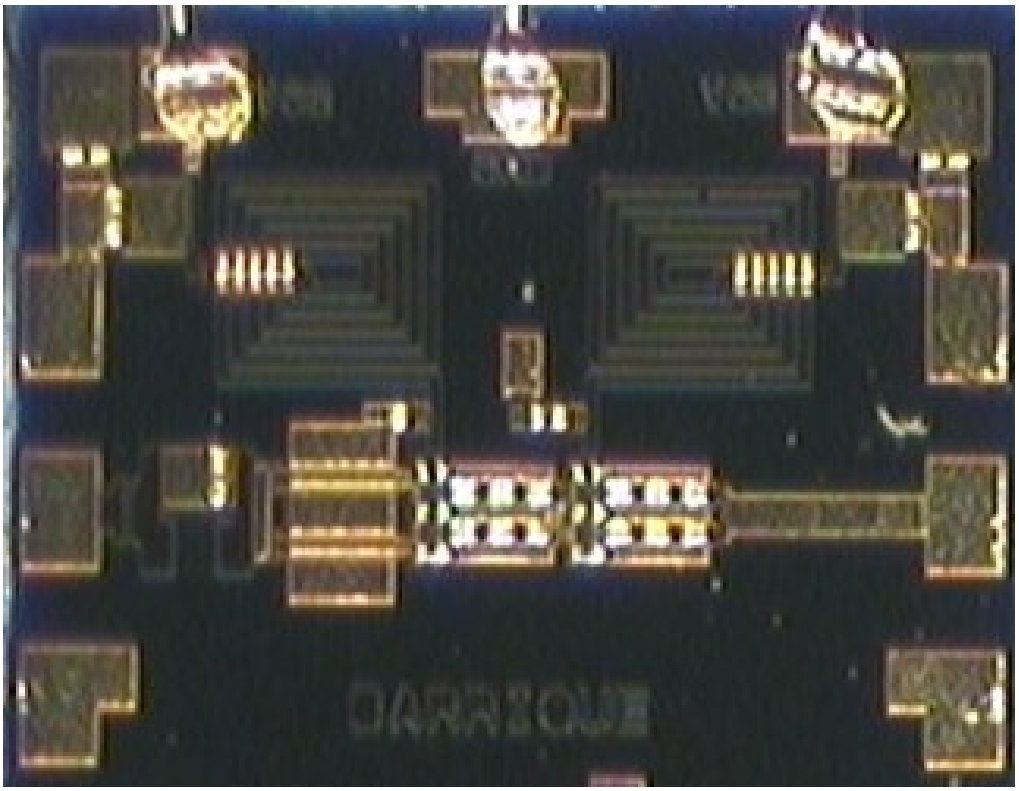
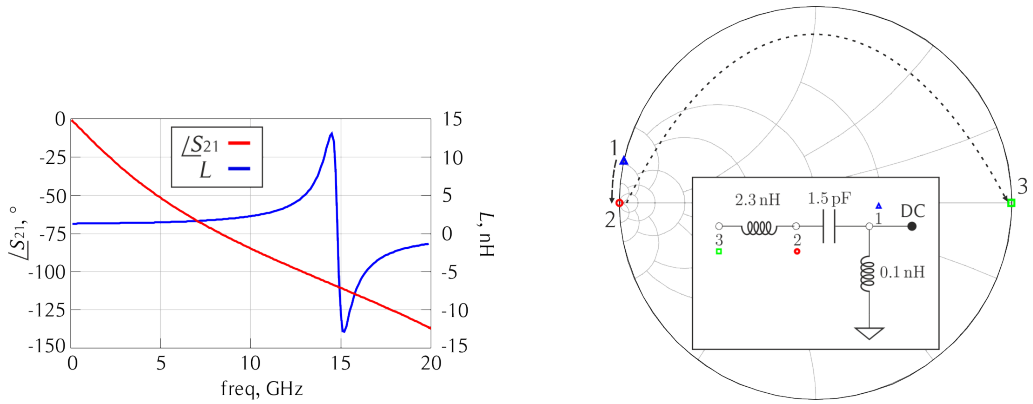


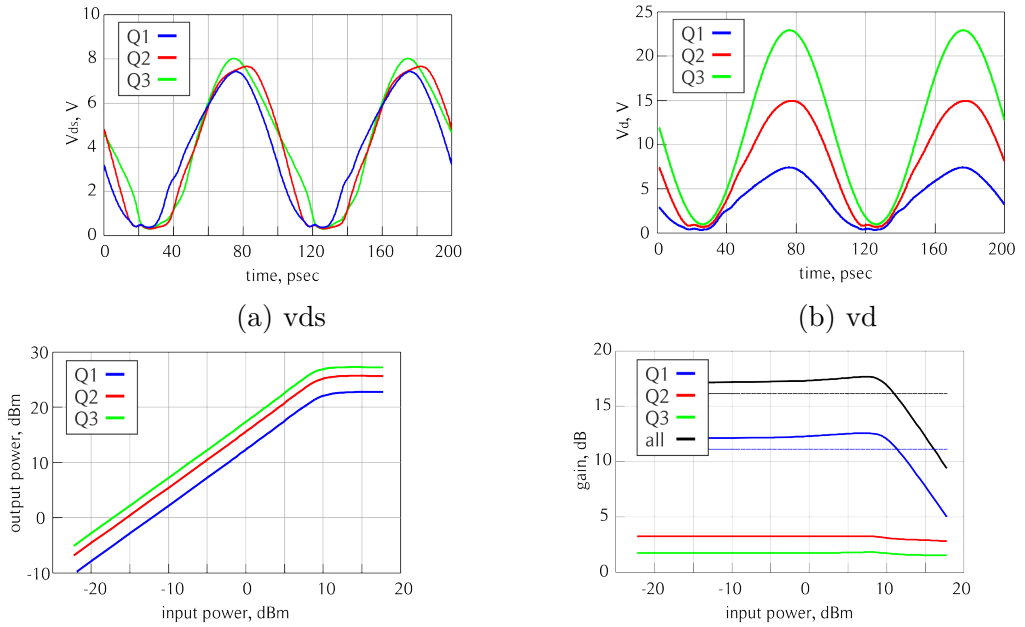
Figure 4.15: Microscope photograph of the realized 3-stage stacked MMIC.



(a) (b)

Figure 4.16: Small signal parameters of the bias inductor (b) and design strategy of the gate bias networks (a).

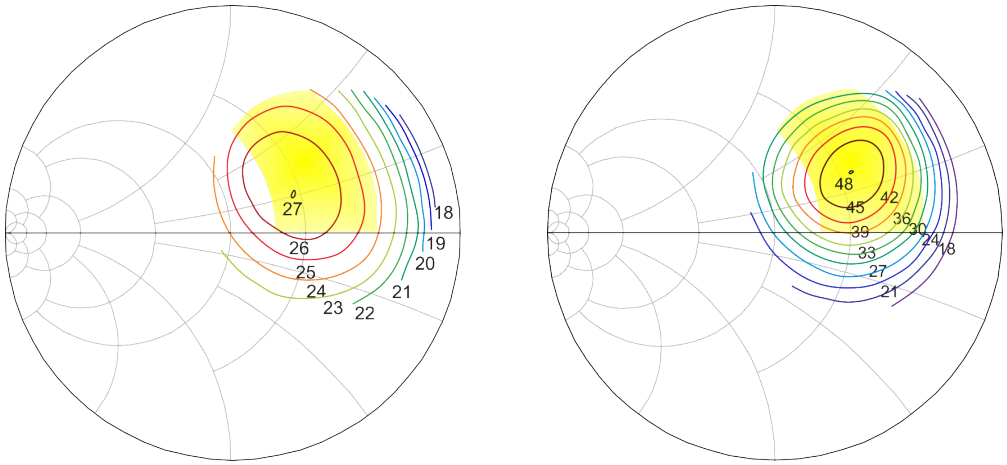
coincide with the theoretical optimum of the MS transistor, despite the two CPW transistors have a slightly different optimum when individually considered. The



(a) vds (b) vd

(c) power (d) gain

Figure 4.17: Performance of the stacked cell loaded by $Y_{\mathrm{d},3} = (8.33 - j3)\,\mathrm{mS}$.



(a) (b)

Figure 4.18: Output power (a) and PAE (b) load-pull contours at 1 dB gain compression.

load yielding highest saturated PAE results to be $(9 - j6)\,\mathrm{mS}$ instead.

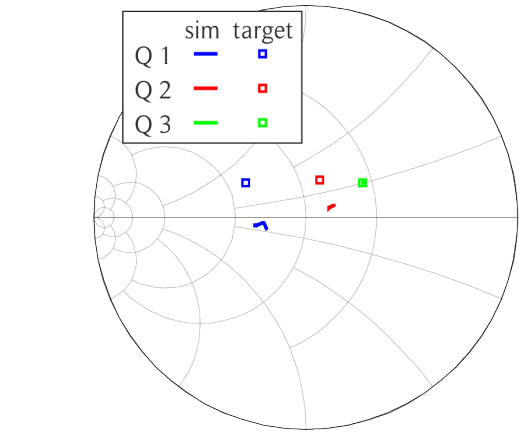
The stack performance in terms of saturated output power, gain and PAE for other relevant loading conditions is summarised in Table 4.2. In particular, the complex loads corresponding to the theoretical optimum for MS and CPW devices have been compared, as well as their real part alone. This allows to determine

Table 4.2: Stacked cell performance for different loading conditions, with harmonics shorted (a) and closed on the same load as the fundamental frequency (b) .

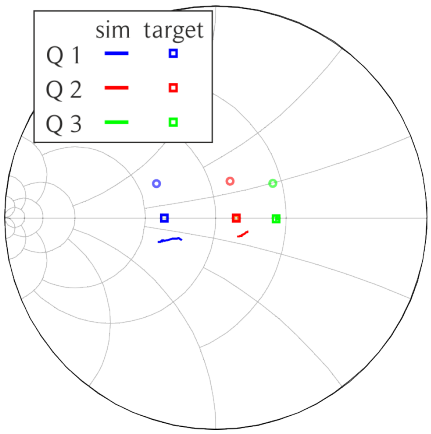
$Y_{\mathrm{d,3}}$ mS	$P_{\mathrm{out,1dB}}$ dBm	PAE_{1dB} %	G_{1dB} dB		
$11 - j4$	27.2 26.8	46 42	16.0 15.8	(a) (b)	MS theoretical opt. for power
11	26 26.1	37 36	15.5 15.4	(a) (b)	real, MS opt.
$8.33 - j3$	27.2 26.3	46 42	16.0 16.0	(a) (b)	CPW theoretical opt. for power
8.33	26.2 25.7	38 35	15.5 16.3	(a) (b)	real, CPW opt.
$9 - j6$	26.8 26.4	48 44	16.5 16.3	(a) (b)	max. PAE, from load-pull
20	23.8 24.3	22.5 24	14.7 14.7	(a) (b)	real, $50\,\Omega$

how critical the role of parasitics is at this specific frequency and, as a consequence, to lead the design of the OMN for a future PA implementation adopting this stacked cell. While a very small difference exists between the $(11 - j4)$ mS and the $(8.33 - j3)$ mS loads, considering the real part only causes a significant degradation, of the order of 1 dB for power and 10% for efficiency. This suggests that, while the assumption of a real optimum load is sufficiently accurate to match the intermediate stages (thus limiting the interstage matching to $C_{\mathrm{g,n}}$ alone), the imaginary part should not be neglected when designing the output matching network to cascade to the last stage. To explain this observation, it is interesting to observe the loading conditions of the three stages when a given load is imposed at the top of the stack. Fig. 4.19 shows the impedance $Z_{\mathrm{d,n,f_0}}$ at fundamental frequency measured at the extrinsic drain of each stage. Fig. 4.19 (f), referring to $50\,\Omega$ load, is somewhat self-standing in that it shows that when the load is far from the optimum value the stacking mechanism ceases to work and the three cells are no longer working in the same condition. This can also be observed in the corresponding case of Fig. 4.20, where the V_{ds} waveforms are shown. Cases (c)–(e) instead, are consistent in showing that the selected design strategy ensures good real part matching of all stages, whereas it presents the first two with a susceptance that is more shifted towards the capacitive side than their optimum would require. In fact, the susceptance of the first and second stages is approximately 4 mS and 15 mS higher than required, respectively. Because this trend repeats systematically for any load value, it is reasonable that imposing a real load on top of the stack worsens the situation, as each stage is loaded with a capacitive impedance that is

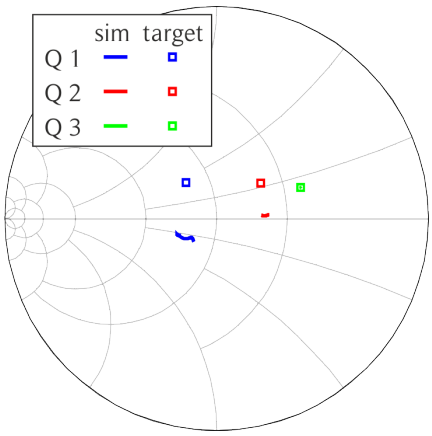
even further away from the optimum one. However, it can also be observed that the real load modulation is preserved when the load $Y_{\mathrm{d},3}$ is varied in a sufficiently narrow range around the design value. In case (e), which corresponds to the optimum for PAE, each stage is still loaded with the appropriate conductance although $C_{\mathrm{g,n}}$ were designed for a different value of $Y_{\mathrm{d},3}$. On the other side, the susceptance is shifted down in a similar way as already observed for the previous cases. Of course, as already mentioned for case (f), when the load is too far from the design value the stack ceases to behave as such and the intermediate stages see an impedance that is significantly far from the ideal one. Additionally, such an impedance becomes more heavily power dependent. Based on these considerations, the range of explored loads for which the stacked working principle is maintained has therefore been identified as the shaded yellow area in Fig. 4.18. This initial analysis based on simulations serves as a guideline to then perform load pull measurements, in which the explored loads should be restricted to values that do not risk to cause too heavy stress or damage to the active devices.



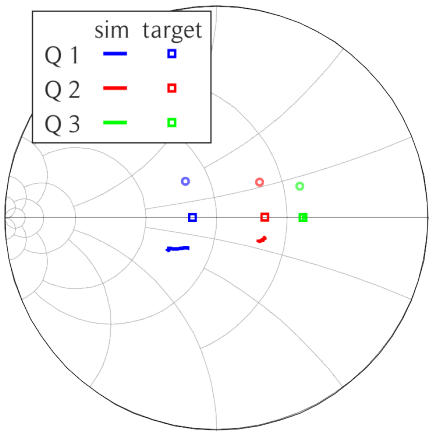
(a) $(11 - j4)\,\mathrm{mS}$



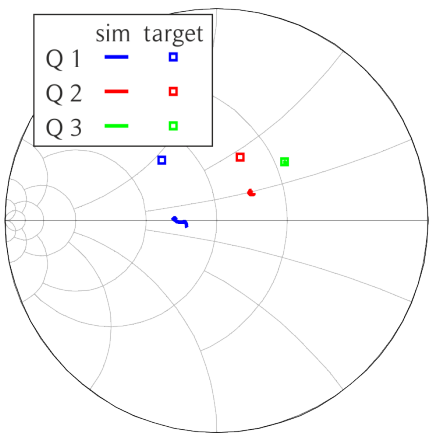
(b) $11\,\mathrm{mS}$



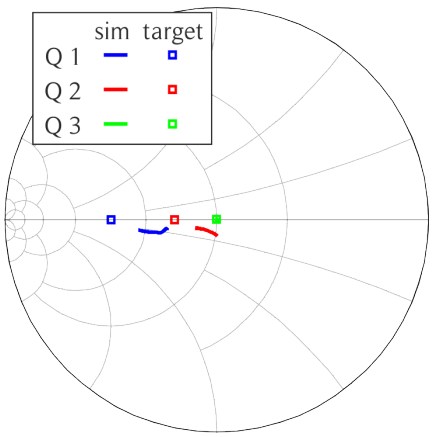
(c) $(8.33 - j3)\,\mathrm{mS}$



(d) $8.33\,\mathrm{mS}$

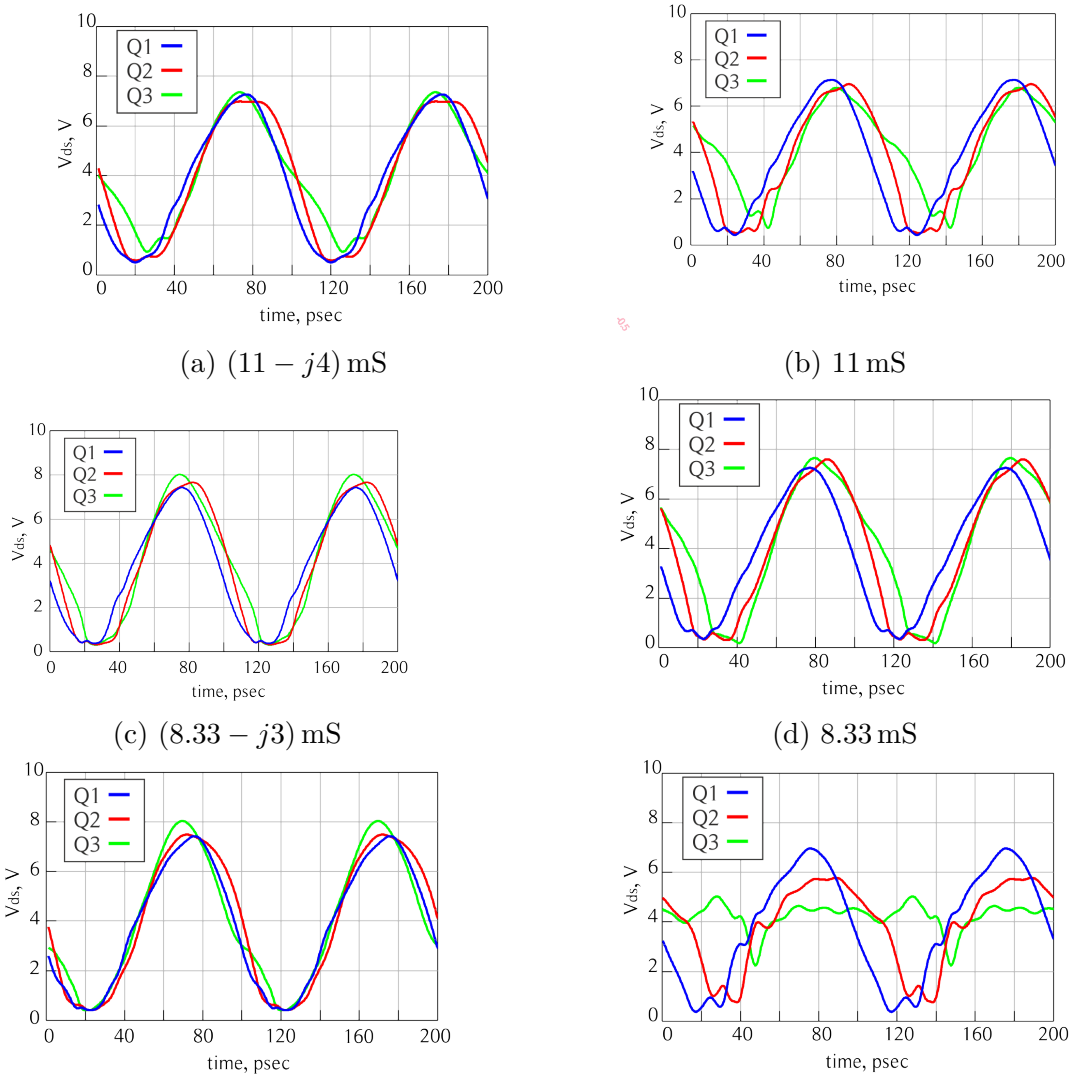


(e) $(9 - j6)\,\mathrm{mS}$



(f) $20\,\mathrm{mS}$

Figure 4.19: Loading conditions of the three stages compared to the theoretical values, for the values of $Y_{\mathrm{d},3}$ listed in Table 4.2.



(a) $(11 - j4)$ mS

(b) 11 mS

(c) $(8.33 - j3)$ mS

(d) 8.33 mS

(e) $(9 - j6)$ mS

(f) 20 mS

Figure 4.20: Drain-source voltage waveforms of the three stages, for the values of $Y_{\mathrm{d},3}$ listed in Table 4.2.

Chapter 5

Conclusions and Future Developments

This work has addressed several open issues in the framework of power amplifiers for wireless communication systems, starting from the circuit and system level and concluding with the device level. The Chireix architecture has been systematically analysed focusing on the bandwidth limiting factors. It has been observed that the device parasitics often represent the bottleneck and some design strategies have been proposed to partially overcome this issue. For instance, absorbing the parasitics into the load compensation rather than resonating them out may lead to some bandwidth enhancement. The design guidelines drawn based on this analysis are applied for the realisation of a prototype, which was presented at the European Microwave Week in 2018 and was awarded the Young Engineer Prize sponsored by the European Microwave Association.
On the other side, the design of Doherty PAs has not been dealt with directly, as the focus was rather on quantifying the advantages of a dual input architecture in an attempt to justify the increase of cost and complexity brought about by its employment in place of the conventional single-input one. Several driving strategies have been presented and discussed, ranging from a totally flexible to a simplified one which permits an almost fully analog implementation. The discussion of these driving strategies is the subject of the works presented at the International Wireless Week and European Microwave Week in 2018.
Concerning these two load modulation architectures, system level experimental characterisation is still ongoing. While an initial assessment of the performance of the dual input DPA under modulated signal has been presented, though based on the simplified driving strategy, the Chireix outphasing architecture requires a more general LUT based approach. This has proven very promising in simulations, but its employment in a real measurement system does present some issue. Some attempts have been done which mainly suffered from phase misalignment as well

as stability of the system calibration in time. Effort is currently being put in overcoming these issues and complete the characterisation of the prototypes, also to assess their linearity.
The study of a further multi-PA architecture that has shown great potential in the enhancement of the back-off efficiency, the LMBA, is also currently ongoing. The design targets the same frequency range as the Chireix and Doherty PAs presented in the previous chapters and is based on the same active devices. After its completion, it will be possible to compare three of the main load modulation architectures.

The two architectures based on load modulation have been realised adopting packaged GaN transistors suitable for S-band operation and power levels of few tens of watts. When higher frequencies are targeted for the same power levels, MMIC realisations are called for. GaN HEMT processes exist that enable the achievement of such performance, but at a significantly higher cost than GaAs pHEMTs, which however have lower breakdown voltages and therefore lesser power capabilities. In this framework, the stacked architecture has been analysed to realise a GaAs multi-transistor structure whose performance is comparable to a single GaN device, at a lower cost. This concept, which is already quite popular in Complementary Metal Oxide Semiconductor (CMOS), is gaining increasing interest for compound semiconductors, though with several challenges both from the stability and from the layout compactness points of view. The concept has been verified by a MMIC cell, designed at a relatively low frequency and meant for source and load pull characterisation. The paper presented at MIKON in 2016. The research thread related to stacked PAs proceeds on a different hierarchical level compared to the first one, as such topology may be applied to any of the above mentioned architectures if these were to be realised in MMIC adopting a low-breakdown voltage technology. Future work may involve the design of stacked cells operating at higher frequencies and the realisation of complex PA architectures, such as but not limited to the ones already explored, based on it.

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